Miniaturization of high frequency power converters

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"If learning the truth is the scientist's goal … then he must make himself the enemy of all that he reads."

Ibn Al-Haytham
965 - 1040

Dedicated to my son Hamza and my daughter Dima

Preface and Acknowledgement

During the past three years, I have had the chance to work in a great place with great people. That place is the electronics group at the Technical University of Denmark.

I would like to thank my wife, my parents, my brothers and sister for supporting me spiritually throughout my life.

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Abstract

DC-DC power converters are major contributors to volume and weight of the most of electronic systems. With the revolutionary development in electronic equipment and added functionality, power converters are required to keep pace with such developments. Therefore, the need for smaller, lighter and more reliable power supply units (PSUs) became a driving force for researchers. To develop such power converters, new semiconductor devices, semiconductor materials, innovative packaging, medium and high frequency (300 KHz – 30 MHz) magnetics, in addition to the development of converter topologies form the pillars for achieving efficient and high-density power conversion. This study represents an investigation of the technological pathways for achieving various levels of integration of power converters. The three major contributions carried out throughout this work are summarized as follows.

First, a study of two semiconductor technologies, which are used in the majority of modern integrated power supplies, is conducted. These two technologies are silicon transistors and gallium nitride transistors. For the silicon semiconductor-based devices, a 140 V power MOSFET with a custom layout is manufactured in a 0.18 µm commercial silicon-on-insulator (SOI) process. The device resistance and capacitances are characterized using a custom designed small signal characterization setup with high voltage bias capabilities. A 32 V class-E resonant boost converter with a self-oscillating gate driver is designed around the MOSFET to test its switching performance at very high switching frequency. The converter is tested at 30 MHz and achieved a power density of 2 W/cm^3.

Second, Gallium nitride FETs are utilized in an 80 V module as well as in a power supply in package (PSiP) achieving a power density of 20 W/cm^3 and an area density of 9.4 W/cm^2. Both versions of the prototypes are tested in the frequency range between 2 MHz and 12 MHz. Air-core solenoid inductors were used in the implementation. The PSiP version of the converter shows a significant enhancement over the module version thanks to the advanced thermally enhanced molding.

Third, Energy storing elements - specifically, inductors and capacitors - are studied aiming for higher density power supplies. Air-core magnetics and printed circuit board spiral inductors are studied. Circular spiral and square spiral inductor structures are implemented and tested in a 10 MHz switch mode power supply. Custom-made Micro-Electro-Mechanical Systems (MEMs) fabricated toroidal inductors in silicon substrates were used to design an 8 V PSiP built on a 3D magnetic-silicon-interposer achieving a power density of 36 W/cm^3. This converter integrates a 3D toroidal inductor in silicon, gallium nitride FETs, gate drivers, input capacitors, and output capacitors, forming a buck converter in 8 mm x 4.5 mm x 1.2 mm volume with a clear path to reduce the profile to 0.6 mm. The converter has a switching frequency of 21 MHz and achieves 83% efficiency. This converter represents an intermediate step for realizing a fully integrated power supply on chip (PwrSoC).

In conclusion, this study represents an exploration of the potential technologies, topologies and methods which have high potential for integration and miniaturization. The study covers

topologies including soft-switching buck converters, Class-E resonant converters, and Class-DE resonant converters. Integrated circuit design technologies including silicon-in-insulator and high-voltage CMOS technologies are used to design two chips. Packaging technologies like module integration, power-supply-in-package, and thermally enhanced epoxy molding are used, not only to achieve tighter integration for the internal components, but also to enhance the thermal and mechanical performance of the prototypes.

Finally, control techniques like on-off control, frequency control, and phase-shift control were investigated to achieve different levels of control for the output voltage or the output current of the power converters. Adaptive dead-time control is identified as one of the most important circuits to integrate in case of applying continuous operation control methods, like pulse width modulation control, frequency control, or phase shift control, as it is a must to use in combination with soft-switching techniques.

With the proper application of the knowledge gained throughout this work, it is possible to achieve high power density converters, and potentially realize the vision of a fully integrated power-supply-on-chip (PwrSoC).

Danish Resume

DC-DC-omformere er vigtige bidragsydere til volumen og vægt i de fleste elektroniske systemer. Med den revolutionerende udvikling i elektronisk udstyr og øget funktionalitet kræves effektomformere for at holde trit med sådanne udviklinger. Derfor blev behovet for mindre, lettere og mere pålidelige strømforsyningsenheder (PSU'er) en drivkraft for forskere. For at udvikle sådanne omformere udgør nye halvlederkomponenter, halvledermaterialer, innovativ emballage, mellem- og højfrekvent (300 KHz - 30 MHz) magnetik og udviklingen af omformertopologier søjlerne for at opnå effektiv og kompakt effektomformning. Dette studie repræsenterer en undersøgelse af de teknologiske veje til opnåelse af forskellige niveauer af integration af effektomformere. De tre store bidrag udført i dette arbejde kan opsummeres som følger.

For Som det første udføres en undersøgelse af to halvlederteknologier, der anvendes i langt de fleste moderne integrerede strømforsyninger. Disse to teknologier er silicium super junction transistorer og gallium nitrid transistorer. For silicium halvlederbaserede enheder fremstilles en 140 V strømtransistor effekttransistor med et specialfremstillet layout i en 0,18 um kommerciel silicon-on-isolator (SOI) proces.

Enhedsmodstanden og kapacitanserne er karakteriseret ved hjælp af en specialdesignet konfiguration af småsignalskarakteriseringer med højspændingsbias. En 32 V klasse-E resonans boost omformer med en selvoscillerende gate driver er designet omkring MOSFET'en for at teste dens ydeevne ved meget høj skiftefrekvens. Omformeren testes ved 30 MHz og opnår en effekttæthed på 2 W/cm3.

Som det andet benyttes galliumnitrid-FET'er i et 80 V-modul såvel som i en strømforsyning i pakke (PSiP), der opnår en effektdensitet på 20 W/cm3 og en arealdensitet på 9,4 W/cm2. Begge versioner af prototyperne testes i frekvensområdet mellem 2 MHz og 12 MHz. Luftspoler blev brugt i implementeringen. PSiP-versionen af omformeren viser en betydelig forbedring over modulversionen takket være den avancerede termisk forbedrede støbning.

Som det tredje studeres energilagringselementer - specielt induktorer og kondensatorer - med henblik på strømforsyninger med højere effektdensitet. Luftspoler og printplade spiralinduktorer studeres. Cirkulære og firkantede spiralspoler implementeres og testes i en 10 MHz switch-mode strømforsyning. Specialdesignede mikroelektro-mekaniske systemer (MEMs) fremstillede toroidale induktorer i siliciumsubstrater blev brugt til at designe en 8 V PSiP bygget på en 3D-magnetisk silicium-interposer med en effekttæthed på 36 W / cm3. Denne omformer integrerer en 3D-toroidal induktor i silicium-, galliumnitrid-FET'er, gate driver, indgangskondensatorer og udgangskondensatorer, der danner buck-omformer i 8 mm x 4,5 mm x 1,2 mm volumen med en klar bane for at reducere profilen til 0,6 mm. Omformeren har en skiftefrekvens på 21 MHz og opnår 83% effektivitet. Denne konverter repræsenterer et mellemliggende trin til realisering af en fuldt integreret strømforsyning på chip (PwrSoC).

Sammenfattende repræsenterer dette studie en udforskning af de potentielle teknologier, topologier og metoder, der har et stort potentiale for integration og miniaturisering. Studiet

dækker topologier, herunder soft-switching buck-omformere, klasse-E resonansomformere, klasse-DE resonansomformere og active clamped flyback omformere. Integrerede kredsløbsdesignteknologier, herunder silicon-on-isolator og højspændings-CMOS-teknologier, bruges til at designe to chips. Pakningsteknologier som modulintegration, strømforsyning i pakke og termisk forbedret plaststøbning anvendes, ikke kun for at opnå en strammere integration for de interne komponenter, men også for at forbedre prototypernes termiske og mekaniske ydeevne.

Slutteligt blev reguleringsteknikker som on-off kontrol, frekvens kontrol og faseskift kontrol undersøgt for at opnå forskellige niveauer af kontrol for over udgangsspænding eller udgangsstrøm af effektomformerne. Adaptiv dødtidskontrol er identificeret som et af de vigtigste kredsløb, der kan integreres i tilfælde af anvendelse af kontinuerlige driftsstyringsmetoder, som pulsbreddemodulationskontrol, frekvensstyring eller faseskiftstyring, da det er en nødvendighed til brug i kombination med soft-switching teknikker.

Med den rette anvendelse af den viden, der er opnået i hele dette arbejde, er det muligt at opnå omformere med høj effektdensitet og muligvis realisere visionen om en fuldt integreret strømforsyning på chip (PwrSoC).

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Chapter 1

Introduction

Electric energy is one of the basic forms of kinetic energies due to the movement of electrons in an atom. Since electricity was discovered, it played an important role in our everyday life. Nowadays, electrically-powered devices are dominating the ways of how humans are interacting, communicating, and doing their work. Electric light, transistors, and the telegraph are highlighted as innovations that changed history [1].
Consumer electronics like computers, smart phone, lighting apparatuses, smart watches, and other devices need some sort of power conversion internally or externally to provide the desired voltage and current levels to the different internal parts of the systems.

1.1 Background and Motivation

Power supplies are main parts of any electronic system. One category of these power supplies are the DC-DC converters. DC-DC converters are deployed in many applications ranging from micro-watt energy harvesters to high-voltage direct-current transmission equipment.

Power electronics circuits' requirements are tightly attached to the application that will be embedded in. The revolutionary development in electronic equipment and the added functionality, power converters are required to keep pace with such developments. Therefore, the need for smaller, lighter and more reliable power supply units (PSUs) became a driving force for researchers [2].

It is a fact that the manufacturing of small power supply units has become a complicated process as it involves expertise in different topics like semiconductor manufacturing technologies, passive elements manufacturing, thermal management, packaging, control and electronic circuits design.

Integration of power supply components is the only way to achieve miniaturization of PSUs. This integration can take several levels. Board level integration was the most common way to integrate the PSU within the application board where the PSU is mainly built up using discrete components. Power supply modules are among the most common ways nowadays for integrating power supplies into an electronics system, thanks to the mass production of such power modules. However, more advanced ways to build a compact power supply unit are power supply in package (PSiP) and power supply on chip (PwrSoC).

In a PSiP, discrete inductors, capacitor, and transformers can be co-packaged with a power management integrated circuit (PMIC). The PSiP can require the incorporation of some extra components on the application board to deliver the desired voltage, current or power to the load. A PwrSoC is a more advanced integration level where the passive components are monolithically or heterogeneously integrated in one semiconductor substrate. Theoretically, higher integration lowers the cost and increases both efficiency and power density

Developing miniaturized PSiP and PwrSoC devices requires miniaturization of the energy storing elements at the first level. Higher switching frequencies, new magnetic structures and materials, advanced capacitor technologies, new semiconductor devices, three-dimensional integration, and new topologies are ways to achieve that goal.

In this work, the focus will be towards developing power supplies for size-critical applications with output power ranging from 1 watt to 30 watts.

1.2 Definitions

- According to the International Telecommunication Union (ITU) [3] and IEEE standards, the high frequency (HF) spectrum is defined by the frequency range of 3 MHz – 30 MHz, while the very high frequency (VHF) spectrum is defined by the frequency range of 30 MHz – 300 MHz [4]. This definition will be used throughout this thesis.
- To define voltage domains, low-voltage power converters will be used to refer to converters with input or output voltage lower than 16 V, while medium-voltage power converters will be used to refer to converters with input or output voltage in the range of 17 V – 99 V. High voltage power converters will be used to refer to converters with input or output voltage in the range of 100 V – 400 V.
- In-silicon passive device is a term refers to a three-dimensional structure imbedded in a silicon substrate and uses -partially or fully- the substrate thickness as a part of the device. On-Silicon passive device is a term refers to any two-dimensional or three-dimensional device that is grown or deposited on top of a silicon wafer.

1.3 Objectives

The objectives of this PhD thesis are summarized in the following four points:

- ***High frequency power semiconductor device technologies.***
  Power transistors and diodes are the heart of the switch mode power supplies. A better understanding of these devices and their driving circuitry is crucial for successful implementation of power supplies. Gallium nitride enhancement mode HEMTs and Super-junction silicon transistors are selected for this study due to their superior performance.

- ***Integrated Passives for PSiP and PwrSoC***
  Passive devices are the largest components in a power supply. Surface-mounted inductor and capacitor technologies are important to achieve high power density converters. For PwrSoC devices, CMOS-compatible in-silicon or on-silicon inductors is a must. It is an objective to demonstrate microelectromechanical systems (MEMS) technology inductors fabricated at Technical University of Denmark in high and very high switching frequency converters.

- ***Integration Techniques and Packaging technologies***
  Packaging of power supplies can be used for casing so that a pick-and-place machine can treat them as standard devices. Selecting a proper molding material as well as the substrate is very important to achieve higher efficiency and increased reliability through introducing heat dissipation mechanism for the internal components.

- ***Investigation of high frequency and very high frequency power supply topologies***
  Power supply topologies are the key for achieving higher power densities. For mid-voltage and high-voltage power supplies switching at high frequency or very high frequency, utilizing soft switching techniques like zero voltage switching (ZVS) or zero current switching (ZCS) is a must. This is not only to achieve high efficiencies but also to avoid converter failure that may result from the excess heating.

1.4 Thesis Structure

The structure of the thesis and related publications are shown in the color-coded figure 1.1. The publications are attached to the thesis as appendixes.

The thesis Introduction, motivation and objectives are summarized in the first chapter followed by a review for the state of the art converters in Chapter 2. Chapter 3 represents a study of two semiconductor technologies which are expected to be used in most of modern integrated power supplies. These two technologies are silicon super-junction transistors and gallium nitride transistors. For silicon semiconductor-based devices, a 140 V power transistor with a custom layout is manufactured in a 0.18 µm commercial SOI process. The device resistance and capacitances are characterized using a custom designed setup. A discussion about diodes for high and very high frequency operation is conducted within this chapter.

Inductors for PSiP and PwrSoC are discussed in Chapter 4. Air-core magnetics and printed circuit board spiral inductors are studied. Circular spiral and square spiral inductors are implemented and tested in a 10 MHz switch mode power supply. This chapter also presents test results of micro-electro-mechanical (MEMs) toroidal inductors in silicon substrates.

Chapter 5 summarizes the topologies used as potential candidates for miniaturization. Starting with soft switching buck converter with switching frequencies of 3 MHz to 22 MHz and input voltages between 5 V and 80 V. Multiple resonant converters topologies are investigated including class-E, class-E derived, and Class-DE designs covers multiple applications with input voltage of 5 V up to 80 V and switching frequencies from 1 MHz to 100 MHz.

Integration techniques and packaging of power modules are discussed in Chapter 6. Two prototypes are discussed in detail. The first prototype is based on module integration of an 80 V soft-switching buck converter using printed-circuit-board (PCB) substrate technology. The second prototype is an 8 V power supply in package (PSiP) using a silicon interposer technology.

Eventually, a summary of all prototypes, in addition to conclusion and future work sections is reported in Chapter 7.

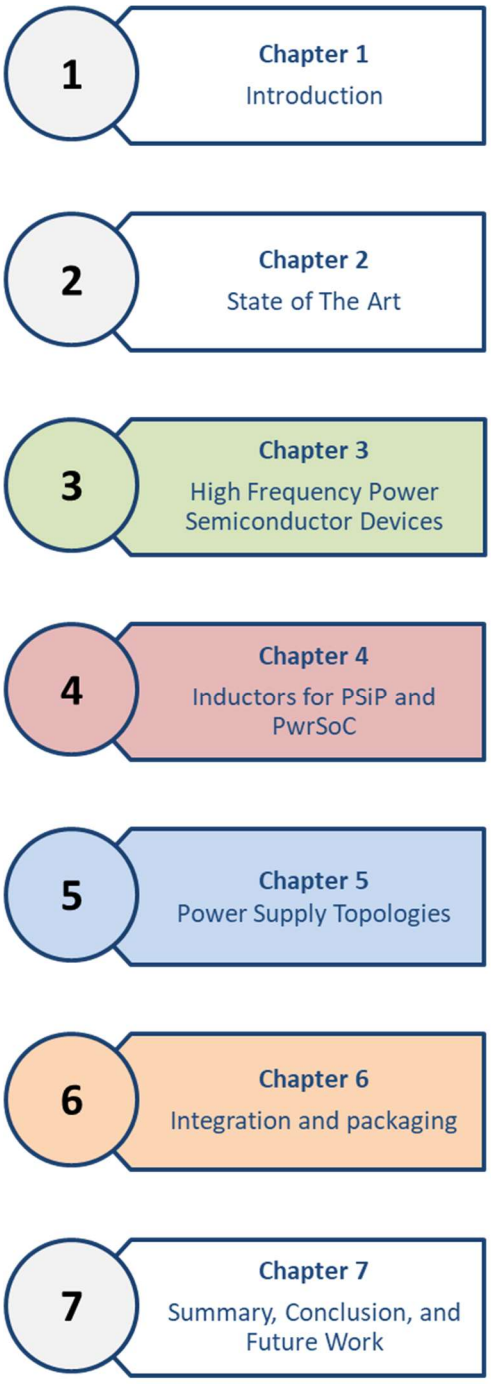


Figure 1.1: Thesis Structure.
Color code links the appendices to the most related chapter

A-Px is referring to a patent application

A-Jx is referring to a journal publication or submitted manuscript

A-Cx is referring to a conference paper or submitted manuscript

Chapter 2

State of the Art

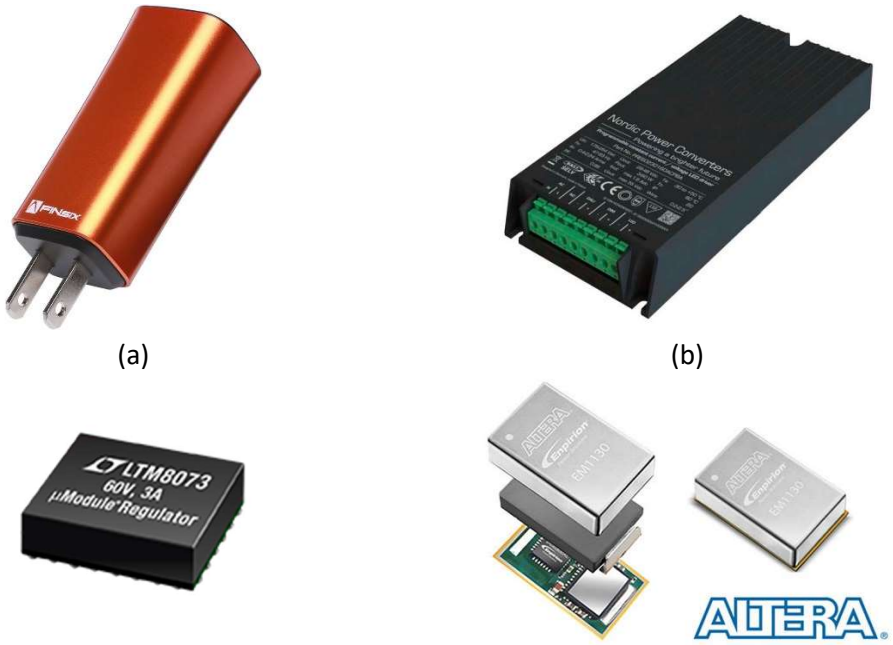
Examples for applications where small size power supplies are needed are LED lighting, Point of load converters for portable devices [5]–[8], Power-over-Ethernet (PoE) equipment [9]–[11], wireless chargers, and DC-DC converters for Internet of things (IoT) [12]–[14].

Point-of-load power supplies for microprocessors and telecommunication systems requires high efficiency and high-power density and recently, shifting power supply input voltages to even higher voltages (48 V) to maximize the power converter chain efficiency added several challenges to the design process. The space available for power supplies is shrinking, merging the space available with high voltage supplies as in [15], [16]

Miniaturized power supply units can be visible to the end customer as product like laptop chargers, smart phone chargers. They also can be imbedded in side electronics devices like laptops, smart phones, smart watches, TV sets or even cars.

Figure 2.1. shows some example for such power supplies where subfigure (a) shows Finsix's DART 65 W laptop charger has a power density around 1.3 W/cm^3 converting 100 – 240 V_{AC} to 18 -21 V_{DC} [17]. Subfigure b shows a 60 W LED driver from Nordic power converters operates from 176-264 V_{AC} to 29-48 V_{DC} [18]. LTM8073 µModule is shown in subfigure (c) which can produce an output voltage of 0.8-15 V from an input voltage up to 60 V and can deliver 3 A continuous to the load [19]. Subfigure (d) shows Altera's Enpirion EM1130 PSiP for high performance FPGA, processor, and DDR memory applications [20].

In this chapter, a review of the state of the art research on integrated power supplies is carried out in section 2.1. followed by state of the art commercial PSiP and PwrSoC converters in section 2.2.



(a) (b)

(c) (d)

Figure 2.1. Examples for the state of the art commercial power converters

2.1 State of the art commercial PSiP and PwrSoC converters

Due to the benefits of miniaturized power supplies in term of weight, size and cost. Many companies are coming up with highly integrated power supplies which incorporates different technologies. In this section, an overview of the state of the art PSiP and PwrSoC devices is discussed in more details.

The focus of this section will be given to extract volume and area power densities as main figures of merits (FOM) for the converters. Summary of commercial integrated supplies is shown in table 2.1. it is clear from the summary that the volume power density is inversely proportional to the input voltage capability of the device. LTM8073 [19] from linear technology is an exception.

For semiconductor device technologies, it is also clear that most of the devices uses silicon MOSFETs in a single or multi-phase buck configuration. For packaging technologies, chip-scale packaging, flip-chip, and wire bonding are used. Three dimensional stacking of the active die on a magnetic substrate is used in [21] and [22]. On the other hand, copper lead-frame is used in [23] which usually has a thick copper. This is beneficial for heat dissipation from the internal components of the PSiP.

A study on commercial products released between years 2003-2008 is reported in [24]. The study provides a large amount of information on PSiP substrates, Assembly technologies, number of components inside the PSiP, Inductor design, encapsulation materials, even the termination finished. A summary of this study is presented in table 2.2. The majority of PSiP in this study shows the usage of epoxy loaded with silica as an encapsulation material. Copper lead-frame, PCB, or a combination are used as a substrate for the converter.

Table 2.1. State of the art commercial integrated PSiP devices and PwrSoC devices

				PSiP					PwrSoC
			Manufacturer	**Fuji Electric**		**Intel (Altera)**	**TI**	**Linear Tech.**	**Ferric**
			Part Number	**FB6831** [21]	**CSM** [22]	**EN2342QI** [23]	**LMZ36002** [107]	**LTM8073** [19]	**PVR** [31]
Specifications	Input voltage		V	2.7-5.5	2.7-5	4.5-14	4.5-60	3.4-60	1.8-3.3
	Output voltage		V	0.8 – (Vin-0.7)	1.2-4	0.75-5	2.5-7.5	0.8-15	0.4-1.6
	Output Current		A	0 - 0.5	0 - 0.5	0-4	0-2	0-3	0 - 3
	Output Power		W	0.9 @ 1.8 V	1	20	15 *	30 *	4.8
	Switching Frequency		MHz	2.5	1.8	0.9 - 1.8	0.2 - 1	0.2 - 3	20 - 120
	Maximum Efficiency		%	90	93.4	94	> 90	> 95	> 85
	Converter's Dimensions	W	cm	0.295	0.35	1.1	1	0.9	0.22
		L	cm	0.24	0.35	0.8	1	0.625	0.14
		H	cm	0.1	0.1	0.3	0.43	0.332	0.025
	Volume Power Density		W/cm^3	127	81.6	75.6	34.9	160	6233
	Area Power Density		W/cm^2	12.7	8.2	22.7	15	53.3	155.8
Technologies	Coil Type			Solenoid	Solenoid	Solenoid	No Info	No Info	No Info
	Magnetic core			Ni-Zn	Ni-Zn	No Info	No Info	No Info	Thin Film
	Capacitor Technology			MLCC	MLCC	MLCC	No Info	No Info	No Info
	Substrate			Magnetic	Magnetic	Lead-Frame	No Info	No Info	Si
	Packaging Technologies			Wire-bonding + Stacking	Flip chip + Stacking	No Info	No Info	No Info	Chip scale packaging
	Switches Technology			Si	Si	Si	No Info	No Info	Si
	Topology			Buck	Buck	Buck	Buck	Buck	Multiphase Buck

* De-rating is applied

Table 2.2. Summary of the study reported in [24]

	Product A	Product B	Product C	Product D	Product E	Product F
Year	2008	2005	2007	2003	2007	2008
V_{IN} range	2.375 - 5.5	4.5 -28	3 – 5.5	4.5 - 14	2.4 – 5.5	7 -13.2
Substrate	Lead-frame	2-layer PCB	Lead-frame	6-Layer PCB	4- Layer PCB	Lead-frame + 4-layer PCB
Assembly Technologies	Direct mounting using solder	Single-Sided SMT assembly + CoB mounting of power and control ICs	Direct mounting using silver epoxy die attach adhesive	Double sided SMT solder assembly	Single-sided SMT solder assembly	Direct mounting using solder for power ICs and Inductor on lead-frame + Single sided SMT
Inductor	Proprietary design with a central core and external winding	Surface mount chip inductor with center winding	Surface mount chip inductor with center winding	Surface mount chip inductor with 2-piece core	External unit with double “E” shaped core	Surface mount chip inductor with center winding
Encapsulation	Epoxy loaded with silica filler particles	Epoxy loaded with silica filler particles	Epoxy loaded with silica filler particles	Epoxy loaded with silica filler particles	none	Epoxy loaded with silica filler particles

2.2 State of the art research on PSiP and PwrSoC

An increasing interest in very high switching frequency converters is detected during the last few years. A 30 MHz PSiP DC-DC converter with a co-packaged micro-inductor in a stacked configuration is reported in [25]. The micro-inductor is fabricated on a silicon substrate. The maximum measured efficiency is 71.7%. The power IC is wire-bonded in ceramic quad-flat-no-leads (QFN) package. Wire-bonding is also used to connect the inductor to the lead-frame of the package. A SEM image of the converter is shown in figure 2.2a.

Figure 2.2b shows a top view of the PSiP reported in [26]. The integration is achieved by realizing a solenoidal inductor using the PCB substrate and multiple bond-wires. Solenoidal inductors are then filled with ferrite epoxy composite glob to form a core. The power IC is fabricated using a 0.5 µm CMOS process and switching at 5 MHz. With input voltage of 5 V and an output voltage of 2.2 V, the measured efficiency was 52%. The low efficiency was due the power MOSFETs losses as they are not optimized for high switching frequency operation.

In [27], A 200-µm thick spiral power inductor in silicon fabricated at a water level sandwiched by two layers of polymer–magnetic powder composite is used a substrate to form a PSiP. Extra layers of copper are added on tom and bottom for routing and enable the usage of the inductor as a surface-mountable packaging substrate. Through silicon vias (TSVs) are used connect the top and bottom copper layers. The converter is shown in figure 2.2c. A buck converter converting an input voltage of 3.3 V to 1.8 V at 500 mA load current achieved an efficiency of 80% when switching at 6 MHz. The converter size is reported to be 3 x 3 x 1.2 mm^3.

A silicon interposer based buck converter is reported in [28]. The silicon interposer integrated a 15-µm thick spiral inductor and a metal-insulator-metal (MIM) capacitor with a thin film $SrTiO_3$ dielectric material. The power IC is fabricated using a 0.18-µm CMOS process. A photomicrograph is presented in figure 2.2d.

A 50 MHz integrated buck converter is reported in [29]. The inductor is realized using lead-frame and bond-wires to form a spiral inductor. The maximum efficiency achieved was 76.8%.

An interposer based, 8-phase, integrated buck converter is reported in [30]. The inductor is fabricated on a silicon substrate. Although the reported work was limited to input voltage of 1.8 V, it is useful to link this work to Ferric's PVR reported in [31].

A Fully monolithically integrated 4.6 GHz DC-DC converter manufactured in a 0.15-µm GaN-on-SiC process is reported in [32]. The converter topology is class -E^2. Although the super-high switching frequency, the converter achieved a maximum efficiency of 48%.

Table 2.3. summarizes some of the state of the art converters reported in the literature between years 2010-2016. It is noted that most of the research work is targeting PwrSoC but, only very few converters exist in the literature which can be called PwrSoC converters.

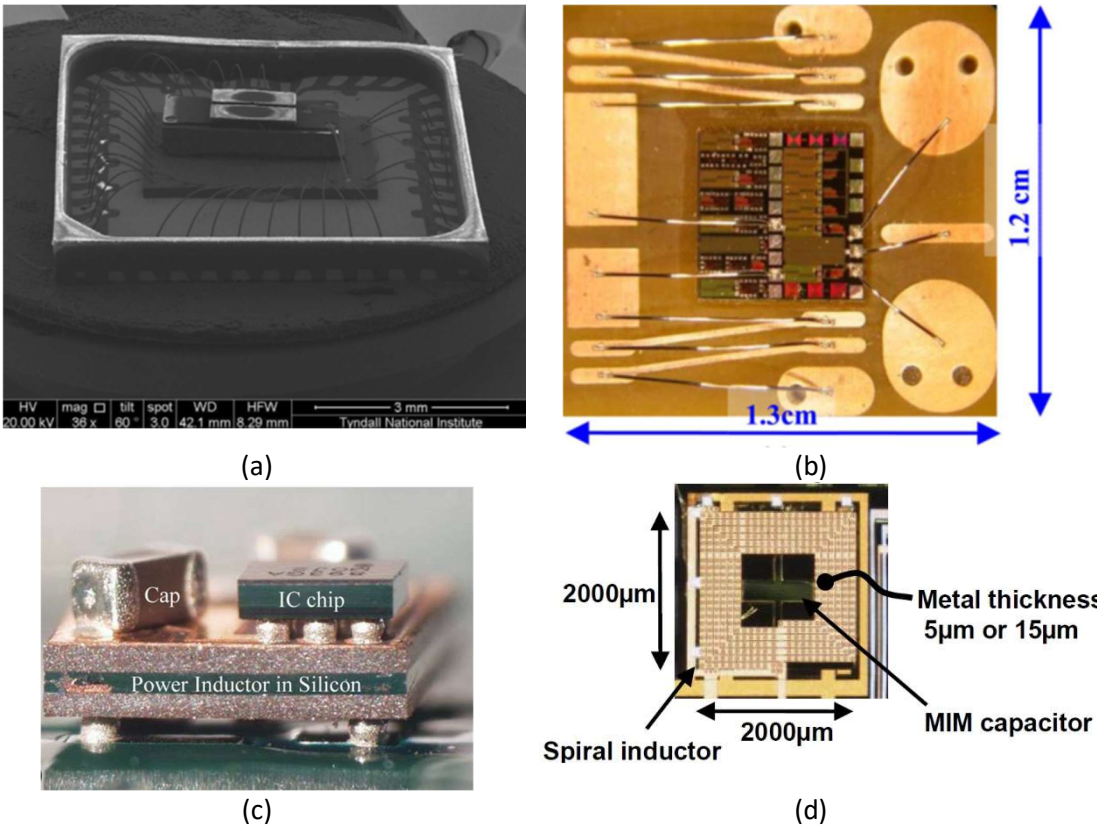


Figure 2.2: A variety of DC-DC converters reported in the literature

(a) SEM image of the PSiP reported in [25] showing the stacked inductor

(b) Top view of the converter reported in [26] before applying the ferrite epoxy glob core.

(c) A photograph of a PSIP reported in [27] using an inductor in silicon as a substrate.

(d) A photomicrograph of the passive silicon interposer reported in [28]

Table 2.3: State of the art PSiP and PwrSoC converters reported in research domain

			Reference	[25]	[26]	[27]	[28]	[29]	[30]	[32]
			Year	2010	2011	2011	2012	2012	2012	2016
Specifications	Input voltage	V		3	5	3.6	1.8	2.5 - 3.3	1.8	8 - 18
	Output voltage	V		1.5	2.5	1.8	1	1.8 - 2	1	1-15
	Output Current	A		0.3	0.12	0.5	0.11	0.25	6.3	--
	Output Power	W		0.45	0.3	0.9	0.11	0.5	6.3	0.2-1.3
	Switching Frequency	MHz		30	5	6	36	50	30-300	4600
	Maximum Efficiency	%		71.7	52	80	76	76.8	71	48
	Volume Power Density	W/cm^3		--	--	83.3	--	--	--	--
	Area Power Density	W/cm^2		--	0.19	10	2.75	--	--	1.37
Technologies	Coil Type			Race-trace	Wire-bonding	Spiral	Spiral	Spiral Wire-bonding & Lead-Frame	Spiral	Serpantin (Hairpin turn)
	Magnetic core			NiFe	Ferrite powder + Epoxy	NiZn powder + PDMS	Si	Epoxy	NiFe	SiC
	Capacitor Technology			MOSCAP	MLCC	Ceramic (MLCC)	MIM ($SrTiO_3$)	MIM	Deep-trench + MOS Cap	---
	Substrate			Leadframe	PCB	Si	Si	Leadframe	Si	---
	Packaging Technologies			Wire-bonding Stacking	Wire-bonding Side-by-side	Flip-chip Stacking	Stacking	Wire-bonding Lead-Frame	Fully integrated	Wire-bonding
	Switches Technology			Si	Si	Si	Si	Si	Si (SOI)	GaN-on-SiC
	Topology			Buck	Buck	Buck	Buck	Buck	Buck	Class-E^2

Chapter 3

High Frequency Power Semiconductor Devices

Power semiconductor devices e.g. field effect transistors (FETs) and diodes are main components in modern switch mode power supplies. The design process for high power density converters is often leads to the selection of high switching frequency due to the advantages in terms of using smaller energy storage elements. For high input voltage converters, a special attention should be given to the selection of suitable power semiconductor devices to achieve a balance between conduction and switching losses. Another source of losses which sometimes dominate the losses in low power converter which is the gate charge related losses.

Parasitic elements play a critical role in the converter performance. For example, MOSFET's gate inductance may lead to substantial voltage ringing. This ringing may cause damage to the MOSFET especially devices designed with thin gate oxide layer.

This chapter discusses power semiconductor devices under high frequency operation. A short review of modern semiconductor materials for power devices is shown in section 3.1 followed by investigation of commercial gallium nitride FETs in section 3.2. A custom layout design of super-junction MOSFET is shown and discussed in section 3.3. A capacitance characterization setup used to test the custom-layout designed device is discussed in section 3.4 followed by FETs and Diodes capacitance assessment using capacitor integral method in section 3.5. A simplified models for diodes and FETs is discussed in section 3.6 and finally, section 3.7 summarizes the design consideration for choosing semiconductor devices for high frequency converters.

3.1 Review of Modern Semiconductor Power FETs and Materials

The development of a controlled power switch started with bipolar junction transistors (BJTs) without latching unlike thyristors. BJTs are suffering from the need of continues base current for control, difficult to parallel, subjective to thermal runaway and second breakdown [33]. The power MOSFETs era started late 1970s enabling higher switching frequencies and triggering the switch-mode power supply development. Superjunction devices concept was introduced for the first time by Shirota and Kaneda to form a multilayer varactor featuring a highly nonlinear capacitance voltage characteristics [34]. Superjunction power MOSFETs and diodes were introduced in the 1980s and 1990s and commercialized by Infineon and STMicroelectronics in the late 1990s with their CoolMOS and MDMesh products respectively [35].

Advances in modern semiconductor power FETs structures and fabrication technologies allowed silicon-based devices to reach their theoretical limits. For further development, new materials and devices structures are needed to enhance breakdown voltages, switching speed and reliability [36]. Wide bandgap (WBG) devices developments have shown promising performance compared to silicon counterparts. WBG devices are still immature. It is predicted that further development will lead to even better devices. Physical characteristics of silicon and main WBG semiconductors are summarized in table 3-1.

Material evaluation are usually performed using several figures of merits (FOMs). The most widely used FOMs are Johnson's FOM, Baliga's FOMs, Keyes FOM and Fujihira's FOMs. A summary of calculated FOMs based on material properties are shown in Table 2.

Johnson's FOM (JFOM) or voltage-frequency product FOM [37] -introduced in 1966- reflects the quality of realized power transistors operating under high switching frequency conditions based on material properties. It can be calculated based on equation 3-1.

$$JFOM = \frac{E_c . v_s}{2\pi} \tag{3-1}$$

Where

E_c is the critical electrical field for breakdown in a specific semiconductor material.

v_s is the saturated drift velocity.

Keyes's FOM [38]-introduced in 1972- considers the thermal limitations on the speed of semiconductor devices. This FOM can be calculated using equation 3-2.

$$KFOM = \lambda . \left[\frac{c . v_s}{4\pi\epsilon_r}\right]^{1/2} \tag{3-2}$$

Where

λ is the thermal conductivity of the material.

c is the velocity of light.

ϵ_r is the dielectric constant of the material.

The low frequency Baliga's FOM ($BFOM_{LF}$) [39] -introduced in 1982- indicates the effect of material properties upon vertical power FETs in terms of on-resistance. BFOM-LF can be calculated using equation 3-3.

$$BFOM_{LF} = \epsilon_r . \mu . E_c^3 \quad (3\text{-}3)$$

Where

μ is the electron mobility of the material.

Table 3.1: Physical properties for different semiconductor materials

Material	Bandgap	Dielectric constant	Electric Breakdown Field	Electron Mobility	Hole Mobility	Thermal Conductivity	Saturated Electron Drift Velocity	Melting Point
	E_g	ε_r	E_c	μ_n	μ_p	λ	V_{sat}	T_m
	eV	-	kV/cm	$cm^2/V.s$	$cm^2/V.s$	W/cm.K	$x10^7$ cm/s	°C
Si	1.1	11.8	300	1500	600	1.5	1	1420
Ge	0.66	16	100	3900	1900	0.58	0.6	937
GaAs	1.4	12.8	400	8500	400	0.5	1	1240
4H-SiC	3.3	10	3000	720	50	4.9	2	2830
GaN	3.4	9.5	3000	1250	850	2.1	2.5	2500
C	5.5	5.5	4000	1800	1200	20.9	2.5	4000

Data collected from [35], [40]–[43]

Table 3.2.: Calculated normalized figures of merits compared to silicon based on data from table 3.1.

Material	Johnson's FOM	Keyes FOM	Baliga's FOMs (LF)	Baliga's FOMs (HF)	Fujihira's FOM (LF)	Fujihira's FOM (HF)
	JFOM	KFOM	BFOM-LF	BFOM-HF	μ_p	λ
	V/s	-				
Si	1	1	1	1	1	1
Ge	0.2	0.26	0.13	0.29	0.39	0.29
GaAs	1.33	0.32	14.57	10.07	10.93	10.07
4H-SiC	20.00	5.02	406.78	48.00	40.68	48.00
GaN	25.00	2.47	670.90	83.33	67.09	83.33
C	33.33	32.27	1325.80	213.33	99.44	213.33

The high frequency Baliga's FOM ($BFOM_{HF}$) is proposed in 1989 [44] to provide a way to evaluate how good the power devices will be when using different semiconductor materials. BFOMHF can be calculated using equation 3-4 [35].

$$BFOM_{HF} \propto \mu . E_G^2 \quad (3\text{-}4)$$

During the past few years, it was reported that many silicon-based devices broke the silicon limit rule. This is due to that the limit of silicon is derived from conventional MOSFET

structures. To assess the effect for modern MOSFET structures like Superjunction devices, another figure of merit can be used. This figure of merit is known as Fujihira FOM which is proposed in 1997 [35], [45], [46] and can be calculated as follows

$$Fujihira's\ FOM_{LF} \propto \mu.\epsilon_r.E_G^2 \tag{3-5}$$

$$Fujihira's\ FOM_{HF} \propto \mu.E_G^2 \tag{3-6}$$

On a device level - regardless of the manufacturing technology, structure, and materials – researchers historically used three different FOMs to compare the performance of switches. These three figures of merit are:

$$FOM_1 = Q_{gtot}.R_{on} \tag{3-7}$$
$$FOM_2 = Q_{gd}.R_{on} \tag{3-8}$$
$$FOM_3 = Q_{oss}.R_{on} \tag{3-9}$$

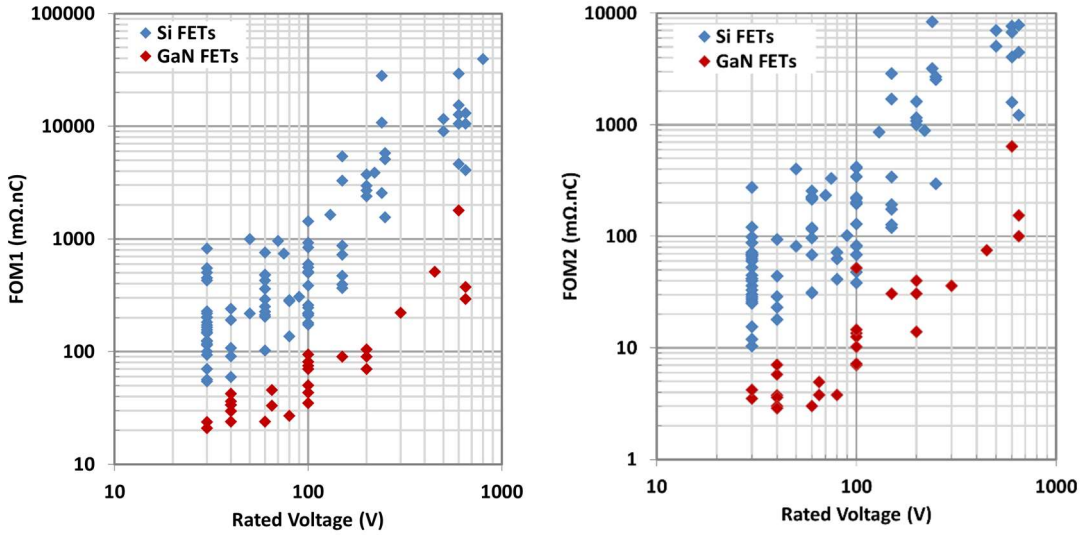
Where

R_{on} is the on-resistance of a power FET
Q_{gtot} is the total gate charge of a power FET
Q_{gd} is the drain to gate charge of a power FET
Q_{oss} is the output charge of a power FET

3.2 Commercial Enhancement-Mode Gallium Nitride FETs

Based on the application, these FOMs –mentioned in section 3.1- are beneficial to pre-judge the performance of a switch in the circuit. For example, in hard-switched SMPS, where the switching loss might be a point of interest. The designer might look at different devices with a comparable on-resistance. FOM_3 is an important parameter to look at for selecting the device with the best performance in terms of switching losses. FOM_2 is important in high frequency applications where the induced dv/dt is crucial to avoid circuit malfunction due to the induced current through C_{gd}. This induced current might lead to false turn-on of the switch causing a shoot-though problem. Depending of the severity of the shoot-though, a reduced efficiency might be the price to pay. In other cases, the switch can be damaged. FOM_1 can be used to compare devices with similar on-resistance in terms of the gate driver loss in case of conventional (hard switched) gate driver. The gate driver loss in this case is dictating the switching frequency limit.

A study was made in [47] -Appendix I- comparing the FOMs for both commercial gallium nitride FETs and commercial silicon MOSFETs at different ratings of drain to source voltage. The results of the study are shown in figure 3.1. which clearly show the superiority of GaN FETs at all voltage levels. Since not all manufactures specify Q_{oss} in the datasheet, it is hard to get accurate information to plot FOM_3.



(a) (b)

Figure 3.1: Summary of GaN vs. Si FETs figure of merits [47], Appendix A-C1.
(a) Summary of high voltage FETs FOM1 ($\mathbf{Q_{gtot}}.\mathbf{R_{ON}}$)
(b) Summary of high voltage FETs FOM2 ($\mathbf{Q_{gd}}.\mathbf{R_{ON}}$)

3.3 Custom Layout Design of Lateral Super-Junction MOSFET

Superjunction FETs break the historical theoretical limits of unipolar devices [48]. The Superjunction concept can be used in many devices such as lateral MOSFETs, Schottky diodes or even IGBTs [35]. Figure 3.2 shows a graphical representation of the specific on-resistance versus breakdown voltage where Superjunction silicon devices project better characteristics compared to traditional unipolar silicon devices above breakdown voltage of approximately 50 V.

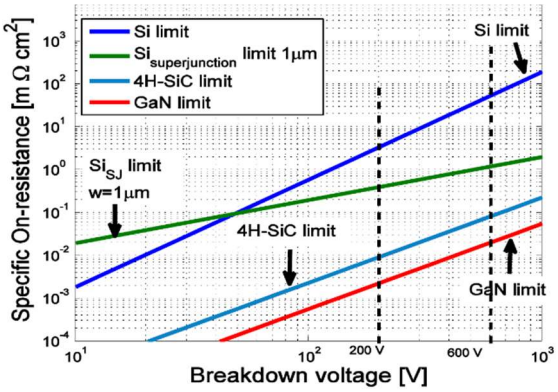


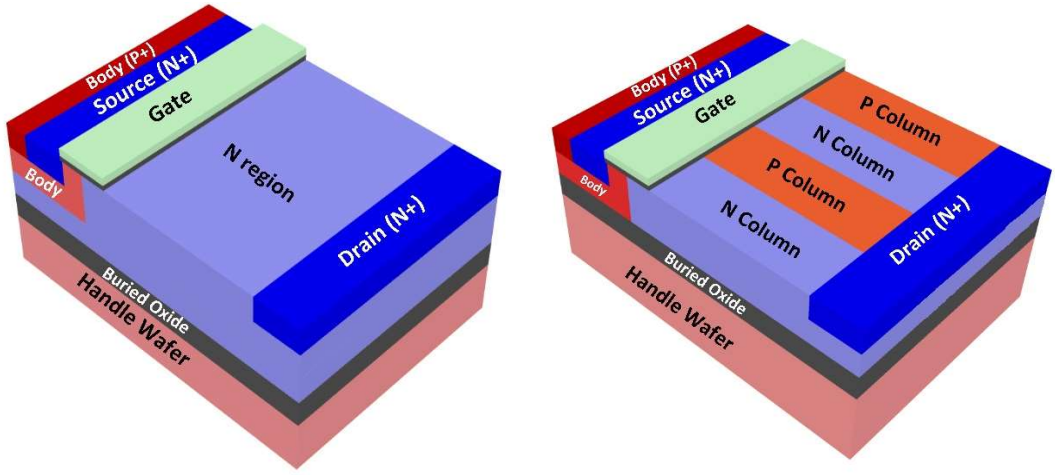
Figure 3.2: Theoretical limits of specific on-resistance versus breakdown voltage for conventional unipolar silicon and wide-bandgap vertical devices versus a Si Superjunction [35].

In general, there are two categories of power devices, vertical and lateral. Vertical devices are formed through the wafer where both sides of the wafer are used as connection terminals of the power devices [49]. So, this technology is suitable for discrete power devices. Some

vertical devices can be constructed in a planer manner where the vertical current is collected by a highly doped buried layer to the top surface of the wafer [50], [51]. On the other hand, lateral power devices can be formed on the surface of a wafer where different flavors of devices can be designed in [52]–[54]. This kind of devices is suitable for monolithically integrated power supplies.

Superjunction MOSFETs were reported by many researchers to have promising performance compared to other MOSFET structures such as lateral double-diffused MOSFETs (LDMOSFETs) – as shown in figure 3.3a – and lateral insulated gate bipolar transistors (LIGBT) [49], [52], [55]. A super junction structure can be achieved by side-by-side or stacked n- and p- regions. This is manly to reduce the peak electric field and make it uniform. This concept allows shrinking the drift regions and achieves smaller devices. A simplified construction of super-junction MOSFET on a SOI substrate is shown in figure 3.3b.

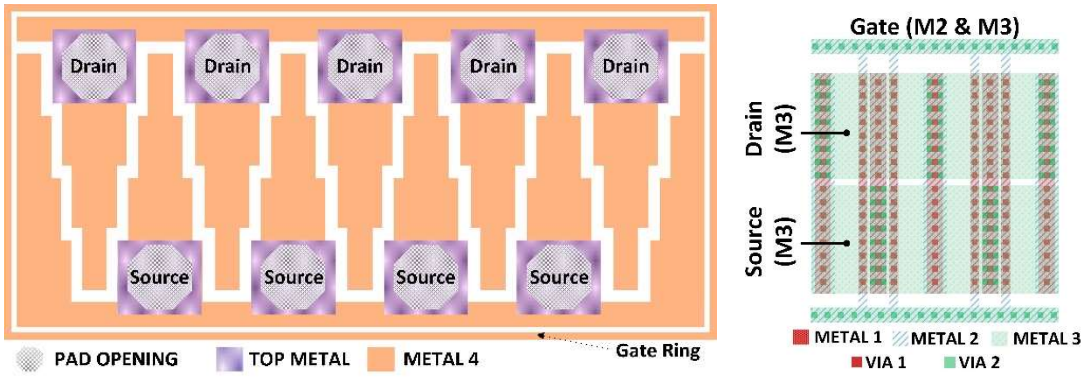
Superjunction device structure is selected due to its better specific resistances (R_{sp}) and enhanced switching performance. For high frequency operation, lower gate resistance, and reduced metallization resistances and inductances have great importance. Metallization structure is designed to assure uniform current flow through the power MOSFET units.



(a) (b)

Figure 3.3: Two different 3D view of high voltage MOSFETs on a SOI process.
(a) laterally diffused MOSFET (LD-MOSFET)
(b) Superjunction MOSFET (SJ-MOSFET)

A multi-finger approach metallization is used, and simplified layout drawings are shown in figure 3.4. Five metal layers are used to construct the connections. The base cell – figure 3.4b - contains metallization from METAL-1 up to METAL-3. At this level all devices located in the X-axis (in the same raw) are connected through METAL-3. The Y-axis drain, and source connections are constructed trough METAL-4. The PAD openings are placed on top of the active device to reduce the routing parasitic elements. The PADs are designed for both wire bonding and stud-bumping rules for flip-chip die attach. A photomicrograph of the manufactured and wire-bonded die is shown in figure 3.5. This device is used for small signal characterization afterwards.



(a) (b)

Figure 3.4: Metallization structure of the power MOSFET.
(a) shows the metallization structure from the bonding pads down to METAL-4. Vias are not shown for easy explanation.
(b) shows the metallization structure from METAL-3 down to METAL-1 for two units of the MOSFET.

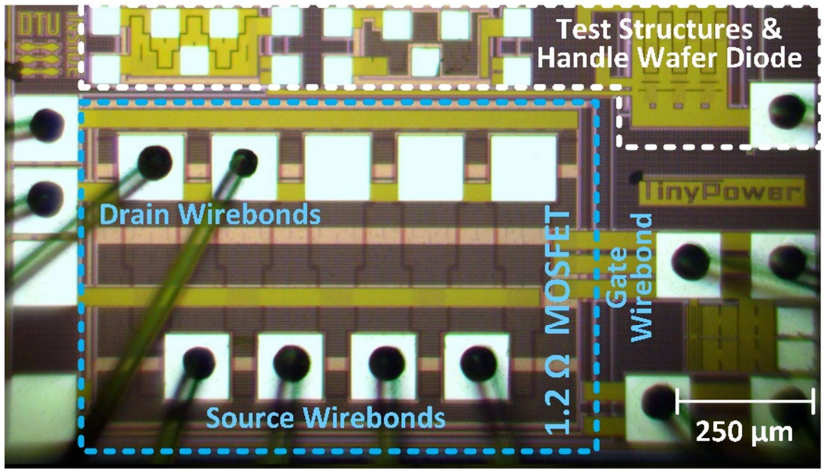


Figure 3.5: A 140 V, 1.2 Ω SJ-MOSFET Photomicrograph (cropped from the test chip)

3.4 Small-Signal Characterization Setup

Semiconductor device's parasitic capacitances can be measured using an impedance analyzer. Some impedance analyzers have an internal bias source, but it usually has a limited voltage range. Furthermore, the impendence analyzer's ports have some restricted voltage ranges for the bias voltage. For example, an Agilent 4294A precision impedance analyzer can source up to 40 V from its integrated voltage source and its ports can handle DC bias voltages up to 42 V.

As it is important to measure device's capacitances and resistances, a custom characterization setup is designed to be able to extract device capacitance under high voltage bias conditions. The setup is built on the idea of using two separated loops for measuring a specific device capacitance. The setup circuit diagrams are shown in figure 3.6 in three different configurations to test output capacitance (C_{OSS}), input capacitance (C_{iSS}), and miller capacitance (C_{RSS}) of a transistor. The guard terminal of the impedance analyzer must be used

when performing in-circuit measurement to reduce the parallel impedance effects which crucial in case of the measurements for C_{RSS}. The guard terminal is the circuit common (i.e. the shield of the all coaxial connectors of the impedance analyzer) [56].

The first loop is the bias loop which is used to set the DC bias voltage – drain to source voltage in this case -. This loop has high AC impedance at the test frequency. The second loop is the test-signal loop that represents an AC coupled port where the impedance analyzer is connected. To measure the input capacitance, and optional capacitor (C3) represents a low impedance for the AC signal to avoid the influence of output capacitance on the measurements.

A generic test PCB design, manufactured, and tested using a reference device. The setup is shown in figure 3.7. The test setup consists of a motherboard and four daughter boards. The daughter boards are designed with a similar layout. Three of the daughter boards are used for calibration (Short circuit, open circuit, and 50 Ω load). The fourth board is to solder the device-under-test on.

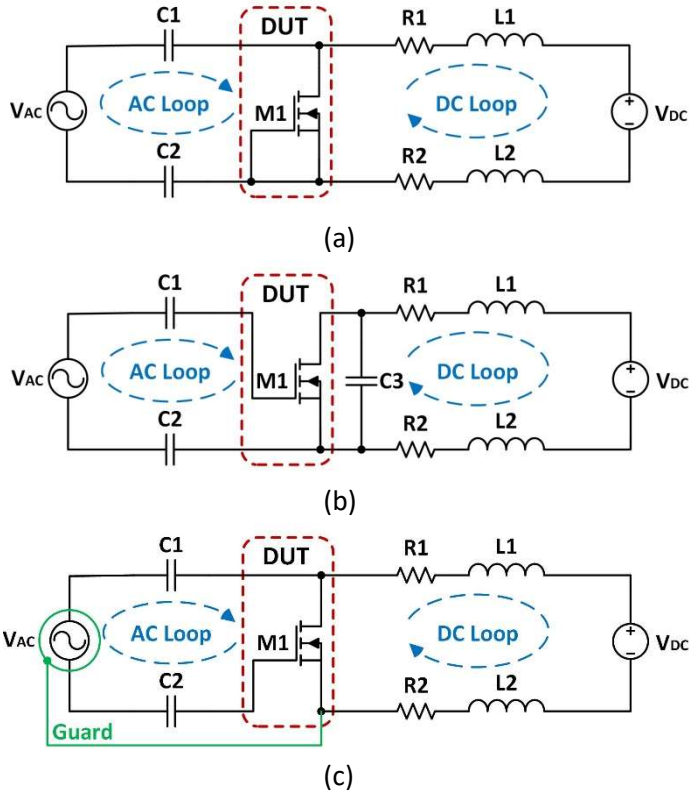


Figure 3.6: Characterization circuits for MOSFET capacitances
(a) Output capacitance (C_{OSS}) measurements setup
(b) Input capacitance (C_{ISS}) measurements setup
(c) Miller Capacitance (C_{RSS}) measurements setup

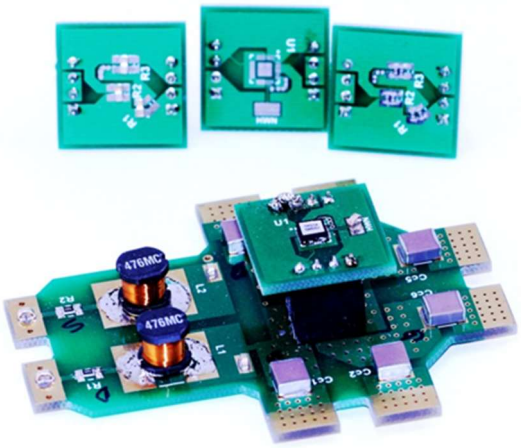


Figure 3.7: Power Transistor Characterization Board
(Together with the calibration daughter boards)

3.5 Semiconductor devices measurement results and assessment

For system level simulation, modeling the non-linear capacitances of diodes and transistors results in prolongation of the simulation time. A linear capacitor may be used in this case by inserting an equivalent capacitance of the non-linear capacitor at the operation voltage.

The value of the linear capacitor can be found by integrating the capacitance curve to obtain the charge as a function of the voltage curve $\mathrm{Q}(V)$. This can be done using equation 3-10. Alternatively, the charge curve can be obtain numerically using equation 3-11 when the characterization data is available and by choosing ΔV to be a small value (10-100 mV) and C_i is the interpolated capacitance value at a specific voltage V.

$$\mathrm{Q}(V) = \int_0^V C(v).dv \tag{3-10}$$

$$\mathrm{Q}(V) = \sum_0^V [C_i.\Delta V] \tag{3-11}$$

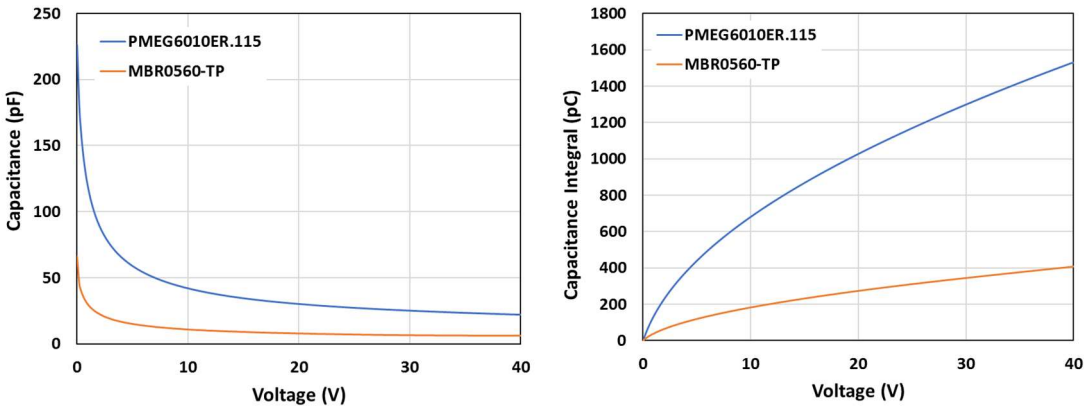
Then, a linear capacitor can be found using equation 3-12 at the operating voltage. The charge curve can also be used to compare diodes.

$$\mathrm{C} = {}^{\mathrm{Q}}/_{\mathrm{V}} \tag{3-12}$$

3.5.1 Diodes

Diode capacitance is a non-linear function of the bias voltage. Figure 3.8 shows the measured capacitance of two 60 V diodes which are used in VHF converters in chapters 5 and 6. The measurements are performed using an Agilent 4294A precision impedance analyzer. The test signal has a frequency of 1 MHz and the bias voltage is swept from 0 V up to 40 V. The resulting capacitance-versus-voltage curve shows a highly non-linear function and shown in subfigure 3.7a. This non-linearity makes it hard for fast assessment of the switching performance of diodes in a certain application. The charge versus voltage curve is extracted using the method presented previously. The PMEG6010ER diode capacitance can be assumed to be 37 pF (1500

pC / 40 V) in system level simulations or calculations during the design phase. On the other hand, the MBR0560 diode can be assumed to be 10 pF (400 pC / 40 V).

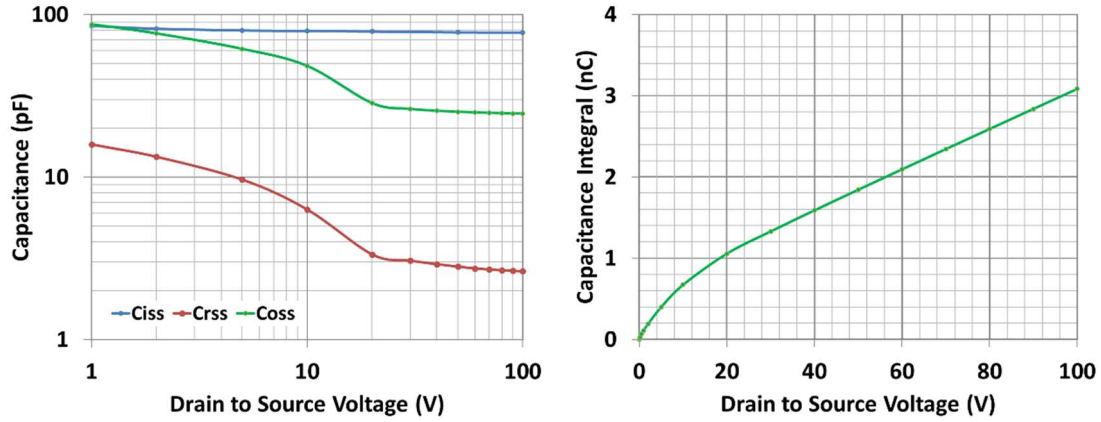


(a) (b)

Figure 3.8: Small signal characterization for two diodes
(a) Capacitance versus voltage curve for two 60 V diodes
(b) Capacitance integral (charge) versus voltage

3.5.2 Transistors

The setup described in section 3.4 is used to measure the Superjunction MOSFET presented in section 3.3. The measurements are carried out using an Agilent 4294A precision impedance analyzer at 1 MHz. The results are summarized in figure 3.9a. The same method of extracting the charge curve is applied to C_{OSS} and the results are presented in figure 3.9b



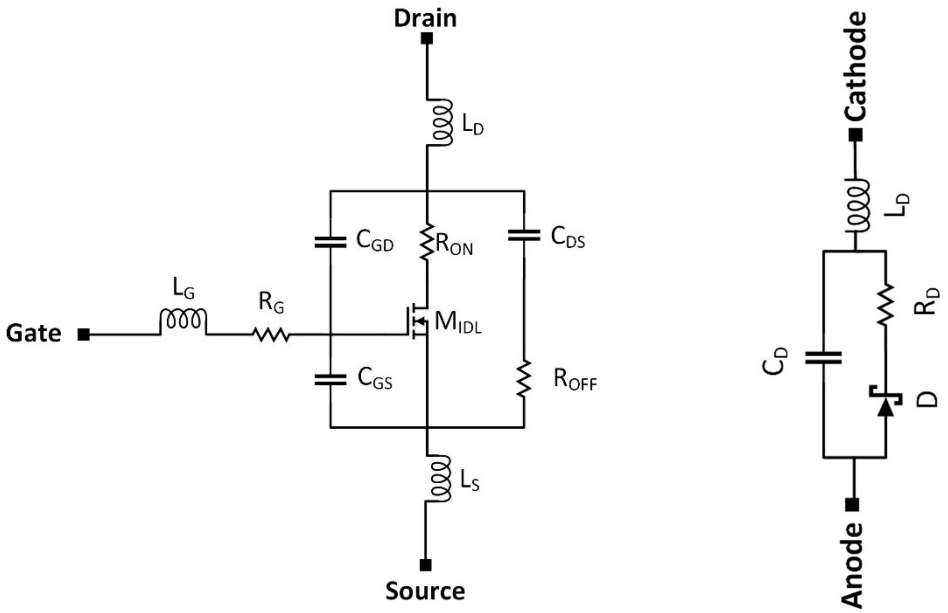
(a) (b)

Figure 3.9. Small signal capacitances measurement results of the fabricated device.
(a)Input, miller, and output capacitances
(b)Calculated output charge as a function of drain-to-source voltage

3.6 Power switch parasitic elements for HF and VHF operation

Simulating switching circuits is a time-consuming process. Therefore, a simplified model can be used to approximate the behavior of a power switch. A simplified model for a power FET is shown in figure 2.10a. The model consists of an ideal FET (M_{IDL}) with a series resistance (R_{ON}) represents the on-resistance. Parasitic capacitances exist between each terminal and the other. R_{OFF} represents the equivalent series resistance of the output capacitance of the FET modeled in series with the drain to source capacitance. The equivalent-series-resistance of the gate R_G consists of the internal gate resistance and other resistances related to the metallization, wire-bonding, other connections of the power FET. L_D, L_S, and L_G are the equivalent-series-inductances of connections between the semiconductor device to the package for drain, source and gate respectively.

Diodes can be modeled as shown in figure 3.10b. Diode series resistance contributes to the conduction losses of a diode. When a diode is used in very high frequency converters, the diode inductance can increase the forward voltage of a diode significantly during switching on the device that leads to excessive losses.



a b

Figure 3.10: Simplified circuit for parasitic elements associated with a power switch

3.7 Summary

This chapter discusses very important components in power electronics converters. A review of power semiconductor materials and devices is presented followed by figure-of merits comparison of two commonly used semiconductor devices, silicon and gallium nitride devices. The emerging gallium nitride power devices technology showed at least one order of magnitude better FOM_1 and FOM_2 for voltages above 100 V. Furthermore, a custom designed layout of a lateral Superjunction MOSFET is presented and device capacitances characterization method and results are reported. The Superjunction MOSFETs are mainly designed as a step towards potential integration of a self-oscillating gate driver-based resonant DC-DC converter [57]–[60]. It is important to mention that custom layout design of power transistors is beneficial to get the right on-resistance and capacitance needed for a specific application.

Based on the study made throughout this chapter, converter design choices are made as follows:

- For HF and VHF converter (3 MHz – 300 MHz),
  - Silicon devices must be combined with a gate driver topology that enables gate charge recovery (e.g. self-oscillating gate driver or any other resonant type gate driver circuits).
  - Gallium nitride devices can be driven using conventional gate drivers thanks to the excellent FOM_1 and FOM_2.
  - For both silicon and gallium nitride devices, soft-switching topologies must be used to avoid failure of the device due to excessive switching losses.

- For medium and lower frequency converter (less than 3 MHz).
  - Conventional gate drivers can be used for both gallium nitride and silicon devices.
  - Efficiency points can be gained by using resonant gate driver topologies targeting higher efficiency systems. On the other hand, complexity of the design increases and freedom of choosing a proper control technique decreases.

Chapter 4

Inductors for PSiP and PwrSoC

Since the early beginning of using switch mode power supplies, it was obvious that the higher the switching frequency, the smaller the converters will be, because of the shrinking size of the energy storage components such as inductors, capacitors. Inductors are by far the dominating components in size and weight. Efficiency and thermal penalties are the limiting parameters for pushing the switching frequency to higher values. To develop such small power converters, high frequency magnetic materials and innovative designs are needed.

This chapter focuses on inductor designs suitable for PSiP and PwrSoC integration. An overview of the state of the art inductor designs is presented in section 4.1, followed by a study of the various inductor designs selected and used throughout the rest of the thesis in section 4.2.

Finally, various custom designs of micro-fabricated in-silicon inductors are discussed for usage in the various prototypes which will be presented in chapter 5.

4.1 State of the art inductors

Inductors for HF and VHF integrated converters can be categorized into three types. The ***first category*** is substrate embedded inductors where the same converter's substrate is utilized to construct the magnetic structure. The substrate can be a PCB, a semiconductor, or even a lead-frame.

Figure 4.1 shows some examples of substrate embedded inductors. An on-silicon 1.2 µH inductor with a race-track winding structure and a magnetic core is shown in subfigure 4.1a. The quality factor of this inductor is 15.1 for a foot print of 50 mm^2 [61]. The magnetic core material is Co-Zr-O. In subfigure 4.1b, a 390 nH thick-copper spiral inductor is manufactured on a silicon substrate and then sandwiched by two magnetic layers made of NiZn powder and polydimethylsiloxane (PDMS) mixture. The quality factor of this inductor is around 10 [27]. A toroidal inductor is silicon is shown in subfigure 4.1c. The 3-D inductors with 25 turns and a diameter of 6 mm achieved a maximum inductance of 60 nH, and quality factors of 17.5 [62].

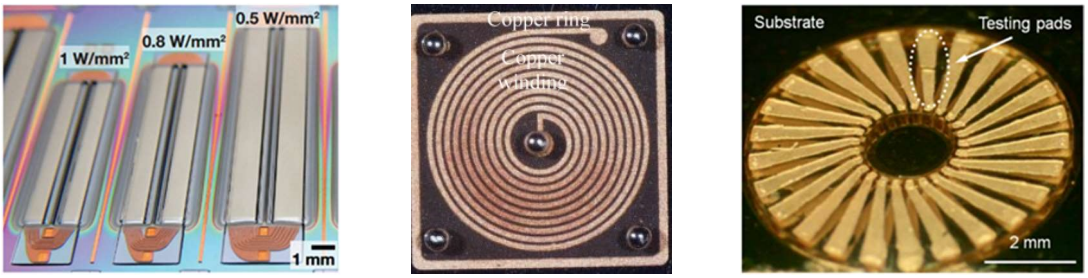
An example of in-silicon toroidal inductors manufactured at Technical University of Denmark is shown subfigure 4.1d. A 44.6 nH inductor achieved a quality factor of 13 with a footprint of 16 mm^2. Variations of this inductor are reported in [63]–[68]. Subfigure 4.1e shows a 4.7 µH 6-layers PCB-integrated inductor windings and core structures in 100 mm^2 footprint. Although the quality factor is not disclosed, the inductor is tested in a DC-DC converter with input voltages up to 7.22 V and delivering 500 mA to the load at 3.3 V. The efficiency of the converter peaks at 71 % and increases to 81 % when the input voltage decreased to 5 V at 1 MHz [69]. Finally, toroidal-shaped inductor embedded in PCBs are reported in [70] in shielded and unshielded configurations.

The ***second category*** of integrated inductors uses the packaging tools and standard materials to form an inductor. For example, different inductors can be realized using wire-bonding techniques. In other examples, a combination of substrate and wire-bonds can be used to form inductors. A lead-frame can also be custom designed to form an inductor as shown in [71].

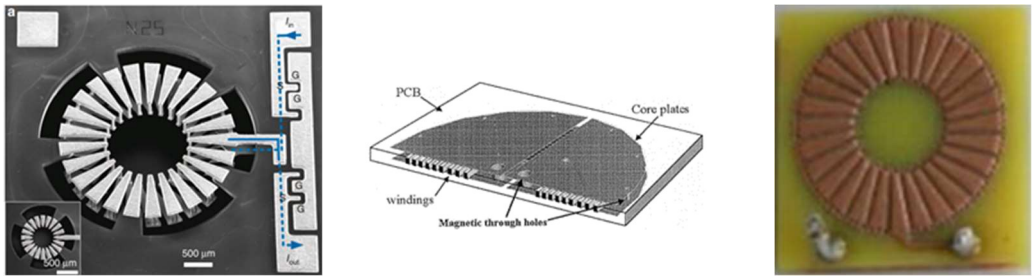
Subfigure 4.2a shows a 4-turn 18 nH square spiral inductor constructed using bond-wires. The inductor is used in a buck converter with an input voltage range of 3 V to 4 V and an output voltage range of 1.5 V to 2.1 V. The switching frequency is between 20 MHz to 140 MHz, achieving a peak efficiency of 65 % when delivering 270 mW of power and output voltage of 1.8 V [72]. Subfigure 4.2b shows a spiral inductor constructed using lead-frame and bond-wires. The inductor is used in a fully integrated buck converter. The maximum efficiency of the converter is 76.8 % for 2.5 V to 1.8 V conversion ratio, while providing a load current of 250 mA and switching at 50 MHz [29]. The lead-frame can be used to realize an inductor as reported in [71] or part of the inductor windings as shown in subfigure 4.2c [73].

Finally, the ***third category***, is surface-mounted discrete inductors (e.g. multilayer inductors [74] or any other discreate inductors) that can be co-packaged with a power integrated circuit to form a PSIP.

In terms of magnetic materials, a detailed study is presented in [75]. A variety of materials can be used for high frequency operation. For example NiFe ,NiZn , NiFeCo, CoZrO and other materials are reported to be used for frequencies higher than 5 MHz.

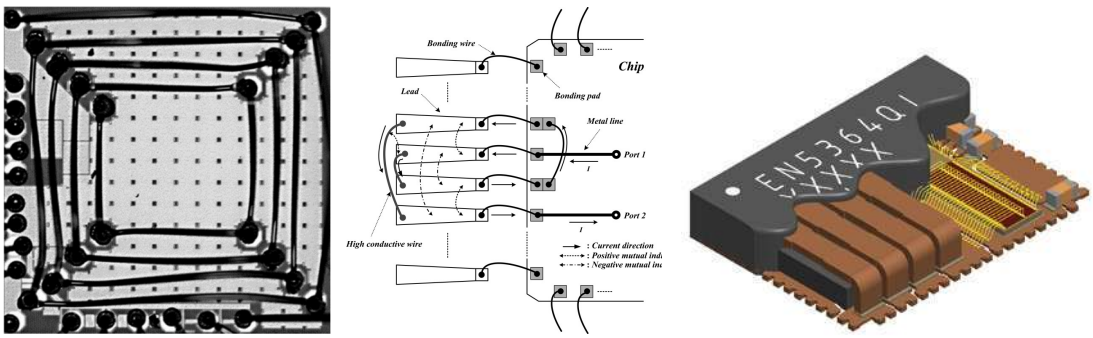


(a) (b) (c)



(d) (e) (f)

Figure 4.1: Examples for substrate-embedded inductors
(a) Race-track inductor structure on silicon [61]
(b) Spiral inductor in-silicon [27]
(c) Toroidal inductor in-silicon [62]
(d) Air-core toroidal inductor in-silicon [68]
(e) PCB-integrated spiral inductor [69]
(f) PCB-embedded toroidal inductor [70]



(a) (b) (c)

Figure 4.2: Examples for substrate embedded inductors
(a) Bond-wires spiral inductor [72]
(b) Combined bond-wires and lead-frame spiral inductor [29]
(c) Lead-frame-based solenoid inductor [73]

4.2 Inductors Selection for HF and VHF converters

In this section, an introduction about the inductor suitable for HF and VHF converters is presented starting from chip inductors followed by ceramic-core inductors. PCB inductors and in-silicon inductors are discussed afterwards.

4.2.1 Chip Inductors

Multilayer inductors are one type of chip inductors heavily used in low-current low-voltage DC-DC converters. For applications like mobile devices, many low voltage rails are required to support the increasing integrated functionality. Multilayer inductors are made by printing electrodes on magnetic sheets and stacking them to form the inductor [76]. This type of inductors can be as small as 1.0 mm x 0.5 mm x 0.7 mm package [77]. Multilayer inductors can be co-packaged with a power IC to form a PSiP. Integration methods can be done by stacking, side-by-side placement or embedding methods as shown in figure 4.3.

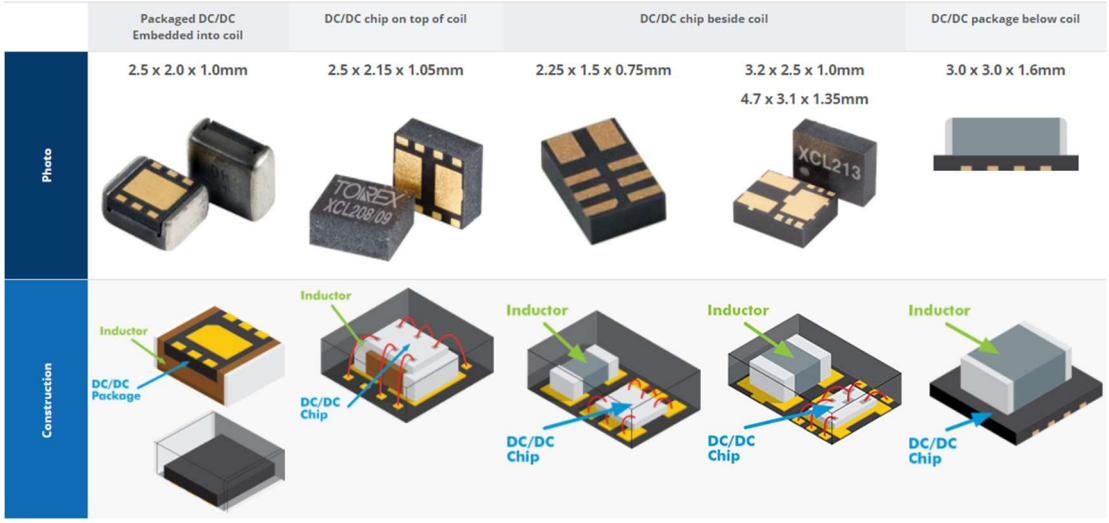
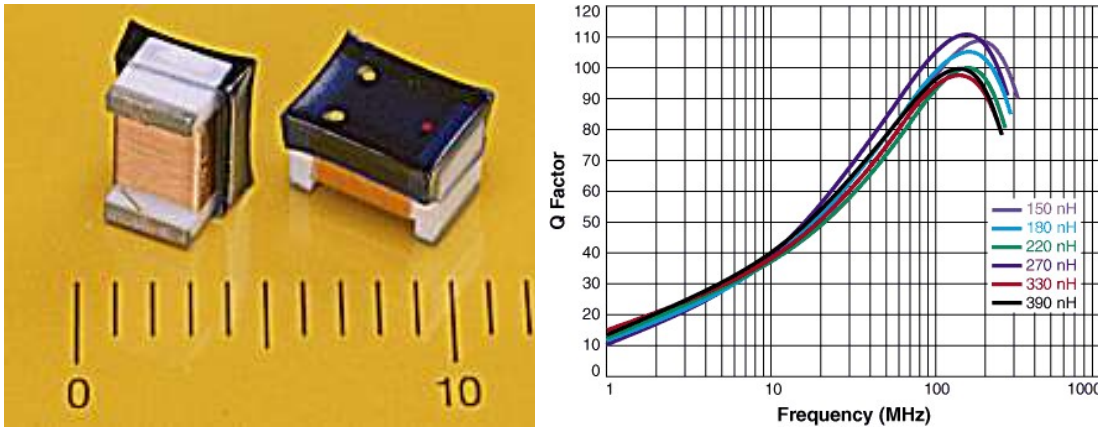


Figure 4.3: PSiP packaging techniques using chip inductors [78]

Although chip inductors have very small sizes, they suffer from high inductance non-linearity, and low-to-medium voltage breakdown [79]. In addition, the magnetic materials used in this type of inductors target hard switched applications where minimized AC current flows in the windings.

4.2.2 Ceramic-core solenoid Inductors

Ceramic-core solenoid inductor are available from different manufacturers. The ceramic core helps the cooling of the winding and enables very high frequency operation. With quality factors above 50 in the VHF spectrum, this type of inductors provides superior performance. Ceramic materials have very low thermal expansion coefficient which makes the inductors more mechanically stable at high temperatures. The mechanical stability also reflects very low inductance variation over temperature.



(a) (b)

Figure 4.4: Ceramic-core solenoid inductors for HF and VHF operation [80]
(a) A photo for ceramic-core inductor from Coilcraft's HA403X series
(b) Typical quality factors versus frequency for Coilcraft's HA403X series

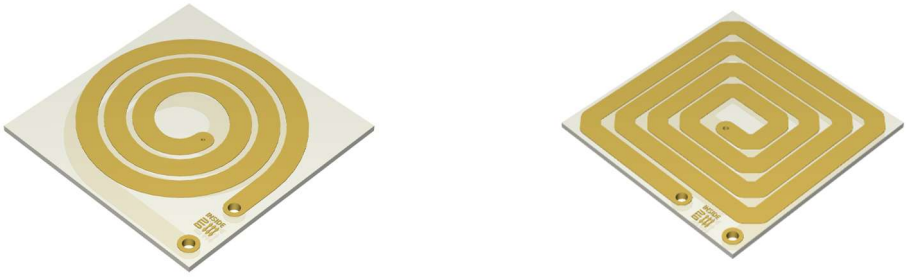
4.2.3 PCB spiral Inductors

Printed circuit board (PCB) spiral air-core inductors can be used in many applications, e.g. RF circuits [81] and power electronics circuits [69], [82]. With the use of multilayer PCB as a substrate for PSIP-integrated supplies, PCB spirals can be used as an embedded substrate inductor. The inductor windings manufactured by PCB machines are more precise and consistent, yielding inductor designs with highly controllable and predictable parasitic parameters [83]. Furthermore, the inductors can be optimized freely to achieve better thermal management, which leads to lower losses [84].

The frequency dependence of a PCB inductor must be considered under higher frequencies. The eddy current effect at high frequencies dramatically increases the resistance of a multi-turn spiral inductor winding. Current crowding is studied through approximate analytical modelling in [85]. Electromagnetic interference (EMI) is also of concern in the PCB air core inductor working under multi-megahertz power converters [86]. Unwanted stray magnetic fields can readily couple to near-by structures. It is well known that the addition of magnetics core plates to either side of the PCB winding provides enhancement of inductance values, and reduction of EMI problem [83].

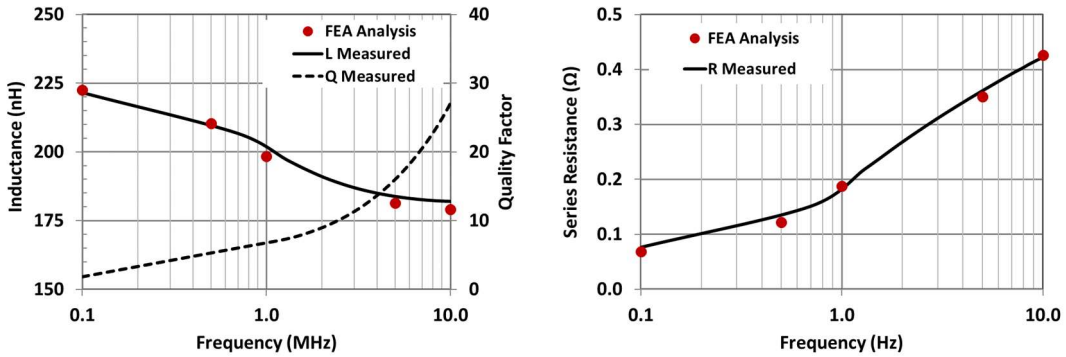
Two spiral inductors were investigated for potential use in a buck converter topology. A perspective view of these to inductors are shown in figure 4.5.

A summary of small signal characterization is presented in figure 4.6 for the ring spiral structure. Characterisation results show a good agreement with the three-dimensional finite-element-analysis-based simulations (FEA) using Ansys Maxwell software. The square-spiral inductor is also characterized and simulated. The results are summarized in figure 4.7. The square-spiral has 75% higher inductance per area and a higher quality factor. More information about testing this type of inductor in a 10 MHz buck converter topology can be found in [87], Appendix A-C4. It is noted also that the designed PCB inductors have comparable quality factors with the commercial ceramic core inductors at 10 MHz.



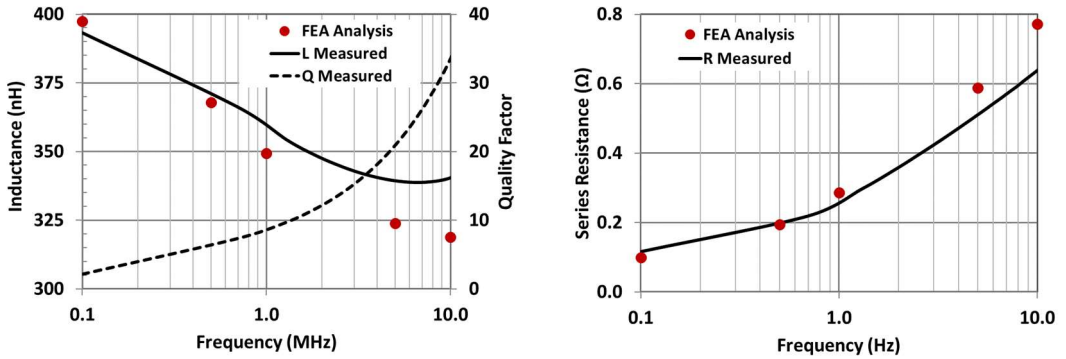
(a) (b)

Figure 4.5: two-layer spiral inductors manufactured on an 80µm thick core flexible PCB
(a) A 12 mm x 12 mm ring spiral inductor
(b) A 12 mm x 12 mm square spiral inductor



(a) (b)

Figure 4.6: Finite element (FEA) simulations and Measurements results of the ring-type spiral inductor.
(a) Inductance versus frequency
(b) Equivalent series resistance versus frequency



(a) (b)

Figure 4.7: Finite element (FEA) simulations and Measurements results of the square-type spiral inductor.
(a) Inductance versus frequency
(b) Equivalent series resistance versus frequency

4.2.4 Micro-fabricated Toroidal Inductors in Silicon

Inductor micro-fabrication technology is a key technology on the way to achieve a fully integrated PwrSoC. A variety of inductors manufactured at Technical University of Denmark is shown in figure 4.8. All the inductors have toroidal structure. The air-core inductor shown in subfigure 4.8a is tested in a VHF converter which will be presented in chapter 5. The silicon core inductor shown in subfigure 4.8b is compared to the air-core inductor in a small-signal characterization setup and in a VHF converter. The test results of the converter show better behaviour, in term of losses, for the air-core inductor. Additionally, two types of core materials were introduced to fill the hollow structure of the air-core inductor to enhance the inductance per area as shown in subfigure 4.8c and 4.8d.

Small signal characterization is performed on the four MEMS inductors and the results for the silicon core and air core are presented in figure 4.9. Both inductors have a footprint of 9 mm^2 and a thickness of 350 µm. Although, the inductance for both devices are almost the same, the quality factor of an air-core inductor is 47 % higher than a silicon-core inductor. The peak of the quality factor for air-core inductors is 13.3 at 33 MHz compared to a quality factor of 9 at 20 MHz for the silicon-core inductors.

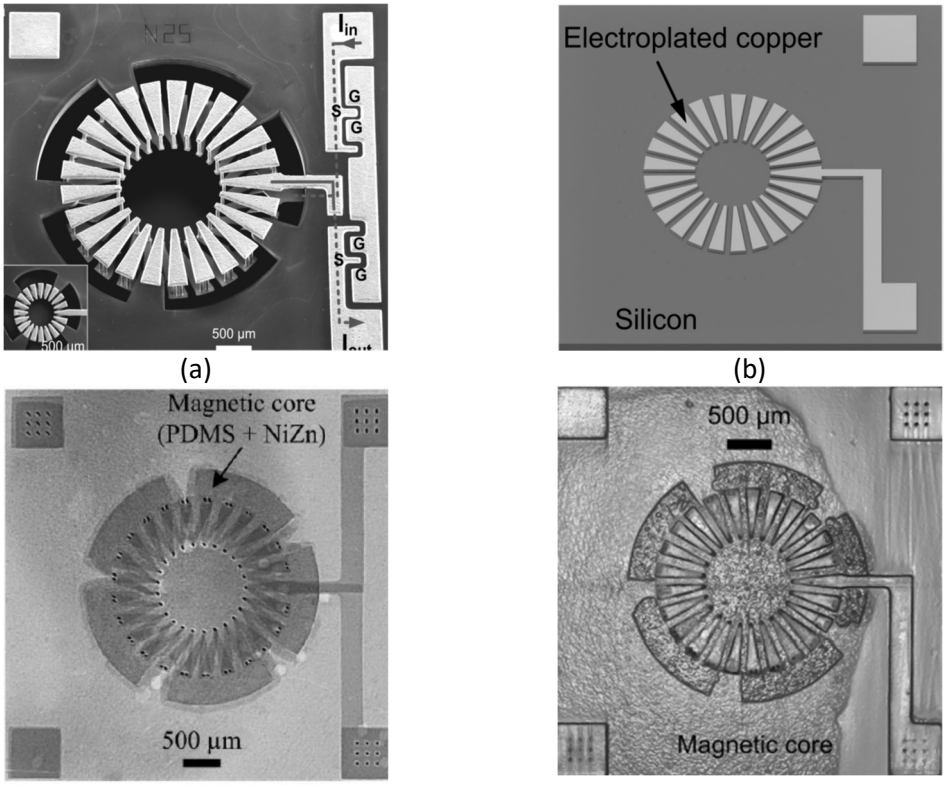


Figure 4.8: Examples of the toroidal inductors manufactured at Technical University of Denmark
(a) Air-core inductor
(b) Silicon-core inductor
(c) Magnetic-core inductor filled with NiZn-PDMS mixture
(d) Novel magnetic core inductor

A smaller footprint (5.6 mm^2) and thinner (280 µm) inductor is filled with NiZn Ferrite material mixed with Polydimethylsiloxane (PDMS) is shown in subfigure 4.8c. In subfigure 4.8d, a small footprint inductor filled with a Novel-material is presented. Small-signal characterization for the NiZn-core inductor is performed and presented in figure 4.10. The inductor has a peak quality factor of 14.3 at 12.5 MHz.

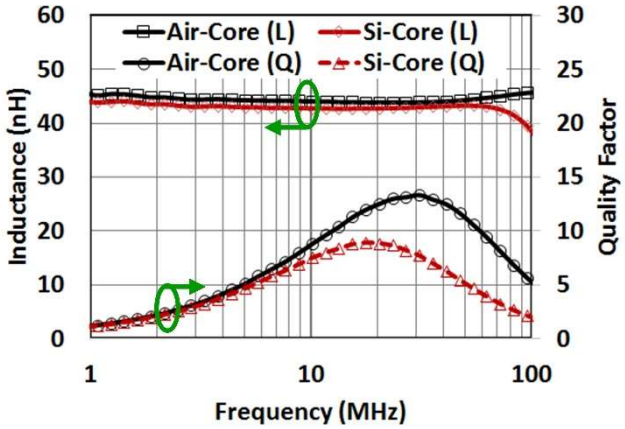


Figure 4.9: Small signal characterization results of the air-core and silicon core inductors.

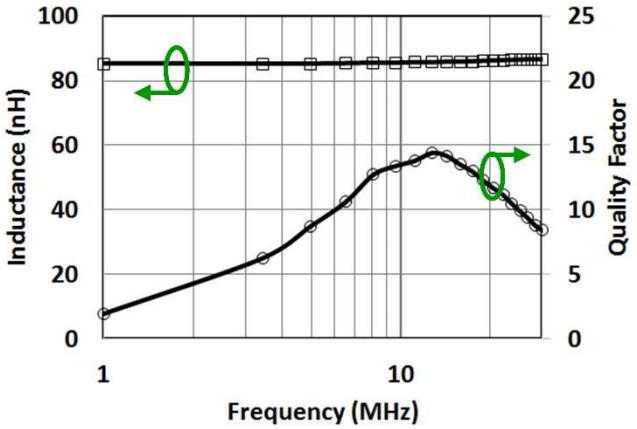


Figure 4.10: Small signal characterization results of the NiZn-PDMS magnetic-core inductor

4.3 Summary

In this chapter, a variety of inductors was investigated for the potential use in HF and VHF PSiP and PwrSoC converters. For PSiP integration, multilayer chip inductors are suitable for low voltage converters integration as reported in the state of the art products in section 4.2.1. For high voltage HF and VHF PSiP converters, air-core inductors (including ceramic-core and PCB embedded inductors) are investigated. A comparison of the designed PCB inductors and alternative state-of-the-art PCB inductors is presented in table 4.1.

MEMS inductors are presented for potential use in PSiP and PwrSoC converters. A variety of sample inductors designed and manufactured in collaboration with colleagues at Technical University of Denmark show promising results. A comparison between DTU inductors and the state of the art inductors is reported in [66] and presented in table 4.2.

A summary of all the MEMS inductors selected for validation in prototypes are presented in table 4.3. A toroidal inductor filled with material-N has slightly lower inductance and quality factors. The main advantage of material-N-based inductor is that it has a stable inductance value versus DC current bias. The inductance changes only by 1.2 % compared to 13.8 % inductance drop for the NiZn-PDMS magnetic core inductor at a bias current of 1.2 A [66].

Design choices based on this study:

- As a part of the resonant circuit, multilayer inductors are not suitable for HF and VHF high-voltage converters, where soft-switching is a must. This is due to their excessive core-losses and limited terminal voltage.
- A suitable application of multilayer inductors in HF and VHF circuits is to be used as a choke, where high inductance is needed, and minimal AC current is passing through the choke.
- Ceramic-core inductors can be used in HF and VHF converters due to their high-quality factors.
- PCB inductors can be used in HF and VHF converters due to their high-quality factor and customizable inductances and footprints.
- Since MEMS inductors have the potential for on die integration, they will be demonstrated in multiple converter topologies depending on the inductance value and the core materials in chapter 5.

Table 4.1: State of the art PCB-embedded inductors at 10 MHz

	Type	L (nH)	Max. Q @ Frequency	Q @ 10 MHz	Thickness mm	Area mm^2
[88]	Toroidal	52	149	10	1.6	222
[89]	Toroidal	240	--	~ 60	1.5	2826
[70]	Toroidal	180	--	--	3.4	48
[70]	Toroidal	165	--	--	3.4	48
This Work	Spiral	223	--	26	0.15	144
This Work	Spiral	393	--	33	0.15	144

Table 4.2: Small-signal performance of TSV air-core and magnetic-core toroidal MEMS inductors compared to the prior works [66].

Study	Inductor geometry	Core material	L (nH)	Q_{peak}@ f (MHz)	R_{DC} (Ω)	I_{SAT} (A)	Footprint (mm^2)	Height (mm)	L density nH/mm^3	FOM
This study	In-Si 3D toroid	Air	32.6	11.5 @ 41.2	0.175	-	9	0.28	12.94	18.37
	In-Si 3D toroid	Air	28.4	8.9 @ 40.9	0.366	-	3.3	0.28	30.74	28.44
	In-Si 3D toroid	C-core*	86.5	14.3 @ 12.5	0.23	1.6	5.6	0.28	54.21	46.36
	In-Si 3D toroid	C-core	112	11.5 @ 12.5	0.265	1.6	5.6	0.28	71.43	44.46
	In-Si 3D toroid	C-core	85.3	11.5 @ 12.5	0.28	1.6	9	0.28	34.01	23.54
	In-Si 3D toroid	N-core**	80.9	13.3 @ 18.4	0.275	4.8	9	0.28	32.10	24.82
UF [105]	In-Si 2D spiral	NiZn + PDMS	390	10 @ 6	0.14	-	9	0.83	52.21	22.34
UF [106]	In-Si 3D toroid	NiZn + PDMS	160	10.5 @ 14	0.265	-	169	0.32	2.96	1.47
HKUST [159]	In-Si 3D toroid	MnZn + PDMS	43.6	16.2 @ 65	0.28	-	2.9	-	-	-
Gatech [69]	In-Si 3D toroid	Air	60	17.5 @ 70	0.191	-	36	0.6	2.78	3.43
Gatech [116]	In-Si 3D toroid	CoNiFe	1000	18 @ 1	0.7	-	100	1	10.00	1.60

* C-core: conventional ferrite core
** N-core: a novel magnetic material
UF: Universityof Florida, USA; HKUST: Hong Kong University of Science and Technology, HongKong; Gatech: Georgia Institute of Technology, USA.

Table 4.3: Summary of Micro-fabricated in-silicon toroidal inductors chosen for the converters presented in chapter 5.

		Inductor A	Inductor B	Inductor C	Inductor D
Publication		[65], [68], [90]	[65], [68], [90]	Appendix A-J1	Unpublished
Converter Topology		Class-E Derived Boost	Class-E Derived Boost	ZVS Buck	ZVS Buck
Winding Structure		Toroidal	Toroidal	Toroidal	Toroidal
Thickness	µm	350	350	280	280
Area	mm^2	9	9	5.6	5.6
Core		Silicon	Air	NiZn + PDMS	Material N*
Inductance	nH	44.6	43.7	85	80.9
Peak Quality Factor		9 @ 20 MHz	13.3 @ 33 MHz	14.3 @ 12.5 MHz	13.1 @ 19 MHz

* Material N is a confidential magnetic material mixed with PDMS.

Chapter 5

Topologies

Seeking integration of power converter is usually lead to the usage of high or very high switching frequency. The selection between hard-switched converters and soft switches converter is no longer a choice at least with medium and high input voltages. This is due to the prohibitively lossy behaviour of power switches when combining both high voltage and high frequency switching.

This chapter summarizes the topologies which are investigated for potential integration in a PSIP or a PwrSoC. The criteria for selecting topologies are the ability to operate in soft-switching regimes, wide input range, and fewer power components count. Four topologies are designed, simulated, tested. These four topologies are quasi-square zero-voltage switching buck converter, high-bridge soft-switching resonant converter, class-E resonant converter, and finally class-E derived boost converter.

A special focus on the emerging gallium nitride FETs and silicon Superjunction along with ceramic-core inductors and MEMS inductors manufactured at DTU.

A variety of converter based on Quasi-Square-Wave Zero-Voltage-Switching Buck Converter topology is summarized in section 5.1 followed by three different types of resonant converters in section 5.2. These three types of resonant converters are class-DE series-resonant converter, Class-E series-resonant converter, and finally, class-E derived boost converter.

5.1. Quasi-Square-Wave Zero-Voltage-Switching Buck Converter

Quasi-Square-Wave Zero-Voltage-Switching (QSW-ZVS) buck converter is a variant of the traditional buck converter – with the same components count – designed to work at high inductor ripple current. A typical QSW-ZVS buck converter schematic is shown in figure 5.1. The inductor ripple current is designed in a way which assures negative inductor current exists at any loading conditions. With an inductor current of a dual-polarity, this current is used to charge or discharge the output capacitance of the switches. The turn-on timing of the switches is adjusted to achieve soft switching.

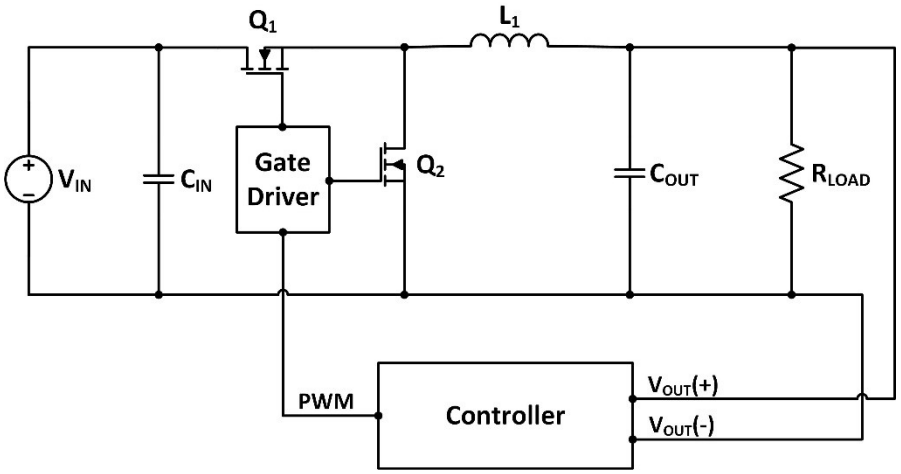


Figure 5.1: A typical buck converter schematic.

Typical QWS-ZVS buck converter waveforms are shown in figure 5.1. the switching period is divided into four subperiods.

- Sub-Period 1 [T1' and T1"]:
  In this sub-period, the low side switch (Q_2) is fully ON and the high side switch (Q_1) is OFF. The switching node voltage equals the voltage drop across Q_2. The inductor current is decreasing less than zero at this period.

- Sub-Period 2 [T2]:
  This sub-period starts when the duty cycle signal forces Q_2 to turn off. The voltage across Q_2 starts to rise due to the negative inductor current is charging its output capacitance and the voltage across Q_1 is falling to zero. When the voltage across Q_1 reaches zero, the Q_1 driver turns Q_1 on.

- Sub-Period 3 [T3]:
  In this sub-period, Q_2 is OFF and the Q_1 is ON. The switching node voltage is equal to the voltage drop across Q_1 subtracted from the input Voltage. The inductor current is rising to its maximum value at the end of duty cycle.

- Sub-Period 4 [T4]:
  The driver forces Q_1 to switch OFF. The positive direction inductor current quickly discharge the capacitances connected to the switching node. The voltage at switching node drops to zero. When the voltage across Q_2 reaches zero, the low side driver forces Q_2 to turn-on.

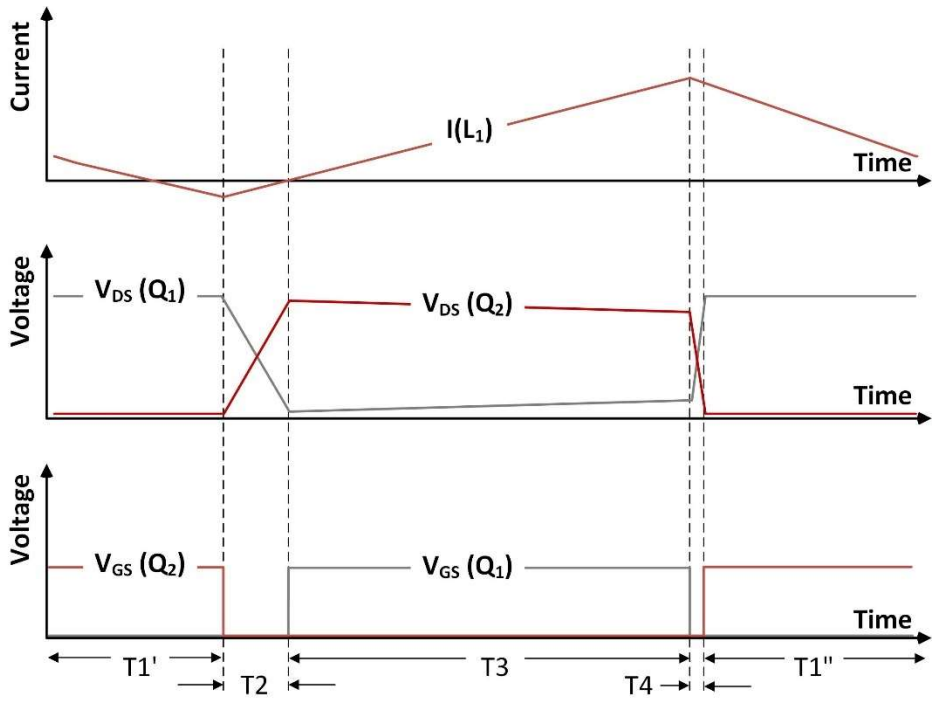


Figure 5.2: Typical Loaded QSW-ZVS Buck converter Waveforms

A variety of buck converter prototypes are designed, simulated, tested, and reported in [47], [87], [91]. This topology is used in the converters summarized in sections 5.1.1 and 5.1.2 where different input voltage ratings and switching frequencies. The topology shows the ability of switching at high frequency and processing energy at medium input voltages at the same time which is not possible with hard-switched buck converters.

It is also noted that this topology requires a special control circuit to optimize the dead-time. This will lead to even high efficiency and improving the thermal behaviour of the circuit.

Conventional pulse-width-modulation (PWM) or burst-mode control techniques can be used to control the output voltage of this topology.

5.1.1 Medium-Voltage Power Stage Module

The power stage is designed to operate at high frequency up to 12 MHz. The module integrates two 100 V rated eGaN FETs driven by a high frequency half bridge gate driver and an air-core inductor. More information about the internal components can be found in [91], Appendix A-C7.

Two variants of the module are designed. Variant 1 uses a 390 nH ceramic-core inductor and is used for input voltages below 60 V. Variant 2 uses 1 µH ceramic-core inductor and is used for input voltages greater than 60 V and up to 80 V.

The circuit is simulated using LTSPICE software. Variant 1 simulation results are shown in figure 5.3. The input voltage for this simulation is 40 V, the output voltage is 13 V, and output power is 12 W. The converter is switching at 7 MHz. The first subplot shows the switching node voltage and the inductor current. A 600-mA negative current can be observed from the simulations which is used to charge the capacitances connected the switching node, mainly the output capacitances of the GaN FETs. The second subplot shows the gate-to-source voltages of the two GaN FETs. As it can be observed, asymmetrical dead-time is introduced to achieve soft-switching operation and minimize the reverse conduction loss, which is similar to body diode conduction for silicon FETs. The power stage simulated waveforms under no-load condition are shown in figure 5.4. In this case, the introduced dead-time is symmetrical and short. This is to avoid extra losses due to reverse conduction for the GaN FETs. It is possible to keep the dead-time fixed and optimized for heavy-load condition, instead of implementing a variable dead-time controller. This will ensure soft switching operation at heavy loads but will result in lower efficiency at light loads.

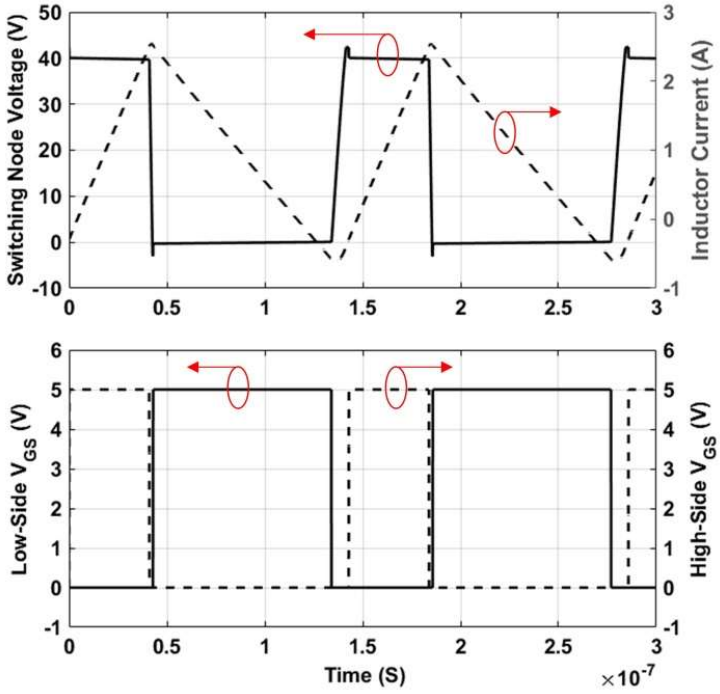


Figure 5.3: Simulated waveforms of QSW-ZVS buck power stage under loading condition and switching at 7 MHz switching frequency.

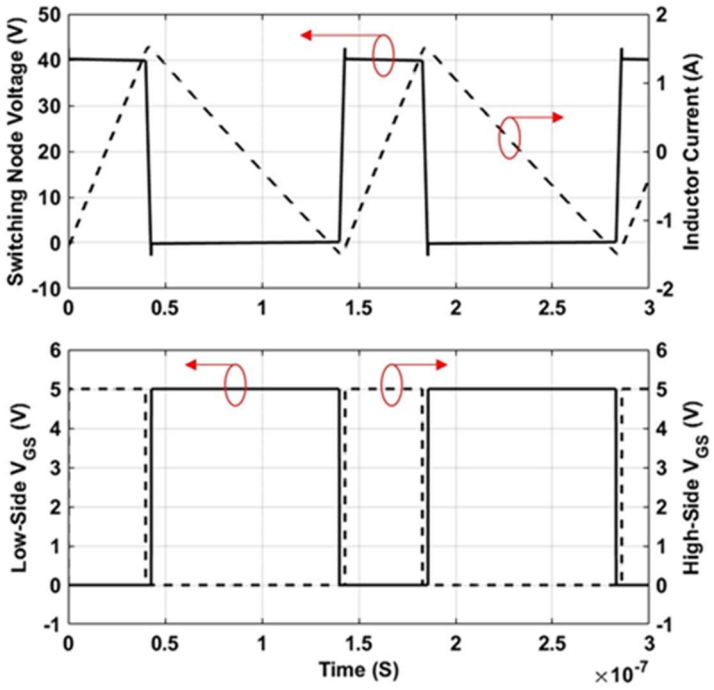


Figure 5.4: Simulated waveforms of power stage under loading condition and switching at 7 MHz switching frequency.

The modules are assembled on high-glass-transition (high Tg) 0.6 mm FR4 substrate. Figure 5.5 shows one of these prototypes where GaN FETs, gate driver, Inductor, Input capacitor and output capacitors are mounted on one side of the substrate. The other side of the substrate is configured to form a 70-pin package for connections to the application board. The finished size of the module is 9 mm x 12 mm x 4.7 mm.

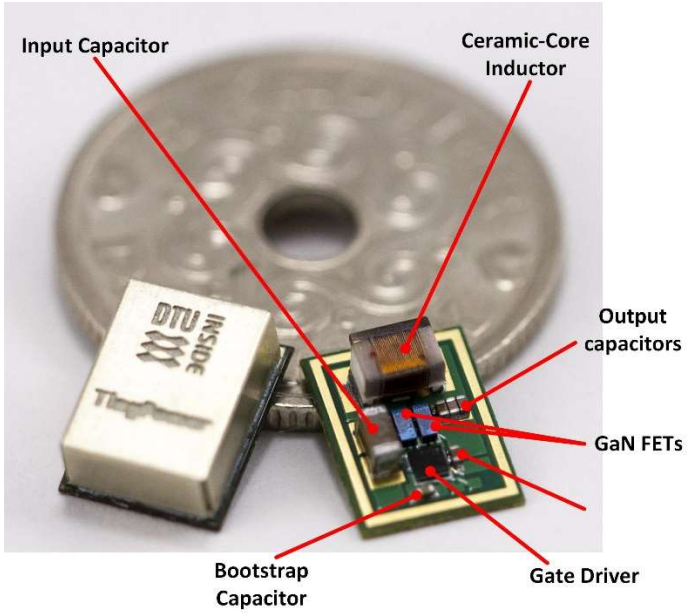


Figure 5.5: QSW-ZVS Buck converter power stage module.

The power stage module is mounted on a test board and the Input signals for the gate driver are supplied via a function generator. The thermal behaviour of the power stage is monitored continuously during the testing. The load is emulated by an electronic load. A thermal photograph of variant 1 of the module at maximum output power is shown in figure 5.6. The thermal image shows a peak temperature of 81.4 ^{O}C on the surface of the inductor. The switches are showing 59 ^{O}, and the gate driver temperature is 65 ^{O}C.

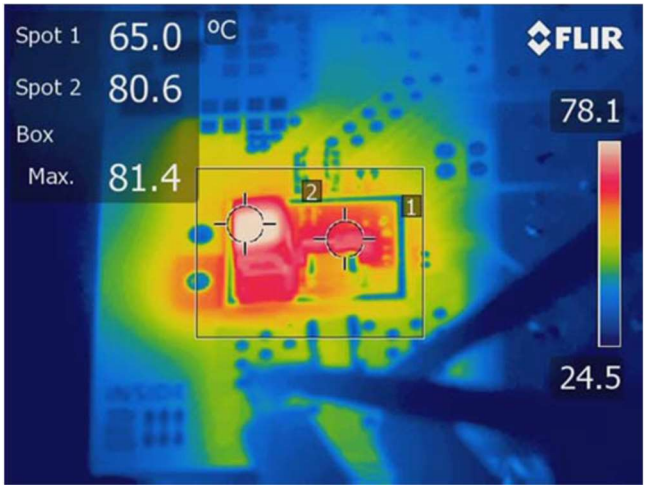


Figure 5.6: A thermal photograph of variant 1 of the power stage module at maximum load.

Efficiency curves is extracted and shown in figure 5.7. for a fixed dead-time circuit optimized at heave load conditions. Variant 1 is used when the input voltage is set to 40 V, output voltage is 14.5 ± 1 V, switching frequency is 7 MHz. Variant 2 is used to when the input voltage is set to 80 V, output voltage is 14.6 ± 1 V, and the switching frequency is 5 MHz. Additionally, variant 2 is tested with input voltage of 60 V, output voltage is 12.5 ± 1.5 V, and switching frequency of 8 MHz. The maximum efficiency measured to be 88.6 %

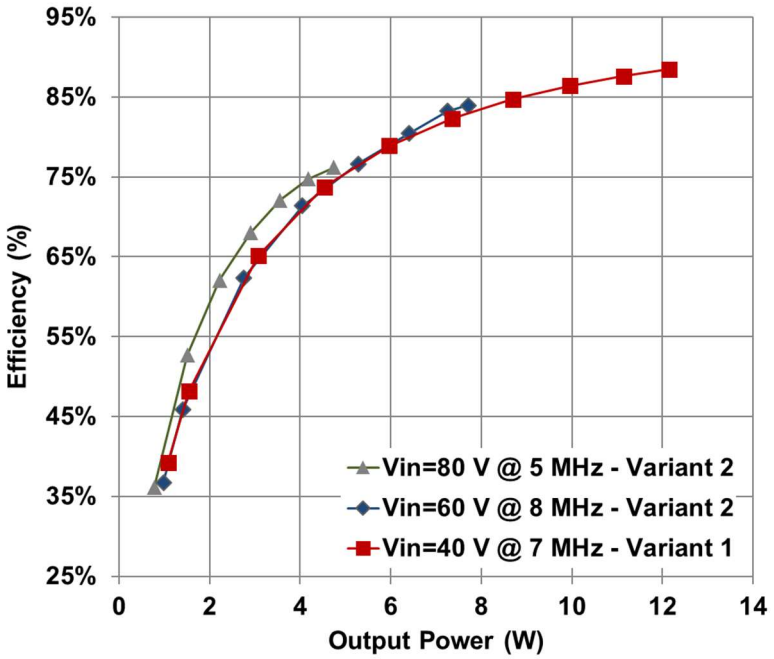


Figure 5.7: Efficiency versus output power of the power stage modules.

5.1.2 QSW-ZVS Buck Converter for large signal testing of inductors.

Testing large-signal behaviour of integrated inductors can be done in two different ways. The first widely-used technique is to use a power amplifier to inject sinusoidal currents into the inductor-under-test and then measure the inductor parameters like equivalent inductance, losses, and power handling capabilities of the device. The second approach is to design a generic setup where the inductor-under-test can be inserted and subject to non-sinusoidal current shapes (triangulate current wave with a DC bias in case of buck converters). The second approach is revealing more about the inductor behaviour with adding the harmonics to the current waveforms. It also gives accurate results on how the device will behave in the final converter.

A. PCB Ring-Spiral Test-Circuit

A 5 W eGaN-based buck converter is designed to test the ring-spiral inductor described in chapter 4. This converter is reported in [87], Appendix A-C4. The converter has an input voltage up to 24 V and switching at 10 MHz. the ring-spiral is then soldered in the circuit and tested with different loading conditions. The converter achieved a peak efficiency of 85% converting a 12 V input voltage to 5 V output voltage and up to 1 A of load current. More results of this converter can be found in Appendix A-C4.

B. MEMS Inductor Test-Circuit

A similar eGaN-based test buck converter is designed to test MEMS fabricated inductors with embedded magnetic cores. This converter is reported in Appendix A-J1. The converter can switch at frequencies up-to 12 MHz with input voltages up-to 24 V.
An enhanced design of the converter is shown in figure 5.8. The enhanced incorporates exchangeable dead-time generation or dead-time automatic control based on board-on-board (BoB) surface mounted assembly technique.

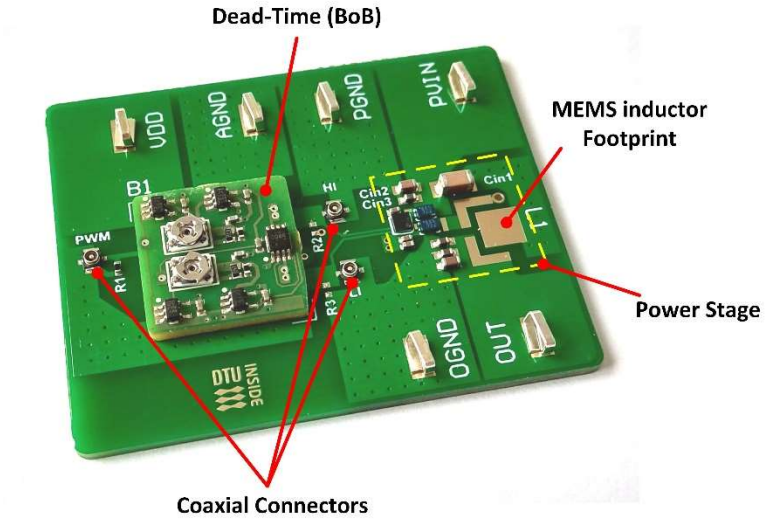


Figure 5.8: QSW-ZVS buck converter for testing MEMS inductors

5.2 Resonant Power Converters

Resonant converters are converters relying on exciting a resonant network to achieve the desired power processing. Resonant DC-DC converters fundamentally consist of three stages a switching circuit, a resonant network and a rectifier circuit. A block diagram of the basic resonant DC-DC converter is shown in figure 5.9.

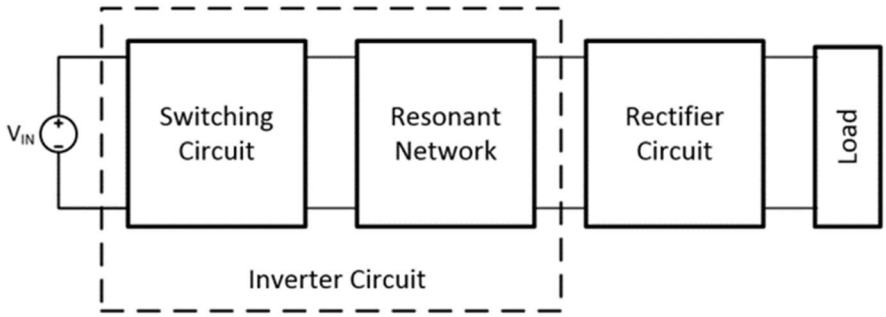


Figure 5.9: Basic block diagram of resonant converters

The first stage the switching circuit- is to convert the DC input to an AC output. The second stage is the resonant circuit which can be modelled as an AC to AC conversion stage. Combining the first and the second stages, results in an inverter circuit which converts a DC input to a desired level AC output. The third stage is the rectifier stage where energy is tapped off the resonant network to feed the output load [92].

Many circuits can be used to implement each one of the three stages. For the inverter circuits, class-D, class-DE, class-E, class-Φ_2, or other inverter circuits can be used. The resonant circuit may also vary significantly from an implementation to another. For the rectifier circuit, many circuits also exist and used in the literature. Class-D, Class-DE, or class E rectifiers are widely used.

An overview of the state of the art resonant converters is summarized in table 5.1. The switching frequency range for resonant converters is extending from hundreds of kHz to multiple GHz [32]. For HF and VHF resonant inverters, a wide variety of semiconductor FETs are investigated. In [93], [94] silicon RF LDMOSFETs are used in a Class-Φ_2 configuration. Si RF VDMOS are used in [78] for implementing a high voltage Class-Φ_2 inverter. Silicon HEXFET devices are used in class-DE [58] and class-E configuration [95]. In [96], silicon TrenchFET is used to realize a Class-Φ_2 inverter. It is also noted, most silicon-based inverters use a resonant type gate driving techniques to recycle the gate-charge to avoid excessive losses in the gate driver circuits. GaN-on-Si FETs are used in [97] to realize a medium voltage a soft switching half bridge LLC inverters. In this case, conventional gate drivers is used benefiting from the superior gate-charge FOM for GaN FETs.

For the rectifiers, Si schottky diodes is dominating the choices reported in the literature even at VHF up-to 110 MHz [93], [94]. SiC Schottky diodes are used in high power rectifiers. Synchronous rectification is used to enhance the efficiency in [96] and [97].

Table 5.1: Examples of the state-of-the art DC-DC resonant converters

Inverter		Rectifier (D = Diode, T = Transistor)			F_{SW}	V_{IN}	V_{OUT}	P_{OUT}	η	Year	Ref.
Topology	**Switches**	**Topology**	**Switches**		**(MHz)**	**(V)**	**(V)**	**(W)**	**(%)**		
Class-Φ_2	Si LDMOSFET	**Class-E**	D	Si Schottky	110	8-16	22-34	23	87	2008	[93], [94]
Class-Φ_2	Si LDMOSFET*	**Class-E**	D	Si Schottky	50	8-18	22-33	17	78	2008	[93], [94]
Class-Φ_2	Si VDMOS	**Class-E**	D	SiC Schottky	30	160-200	33	190	84	2010	[108]
Class-DE	Si HEXFET	**Class-DE**	D	Si Schottky	29	110-150	40	13.4	85	2014	[58]
Class-DE	Si HEXFET	**Class-E**	D	Si Schottky	30	50	5	1.53	83	2013	[109]
Class-DE	eGaN FETs	**Class-DE**	T	eGaN FETs	5	36-44	12	96	89.4	2014	[97]
Class-E	Si MOSFET	**Class-E**	T	Si MOSFET	35.6	14	7	5	80	2015	[57]**
Class-Φ_2	Si TrenchFET	**Class-E**	T	Si TrenchFET	10	16-21	5	10	82	2016	[96]
Class-E	Si HEXFET	**Class-E**	D	Si Schottky	1	5	12	0.5	75	2016	[95]
Class-E	Si HEXFET	**Class-E**	D	Si Ultrafast	0.5	5	3.3	2.5	59	2016	[95]

*** Custom Design 50 V LDMOSFET**

**** Bidirectional VHF Converter**

5.2.1 Class-DE Resonant converter using eGaN FETs

This section summarizes the work done to implement a high-frequency soft-switching half-bridge series-resonant DC-DC converter using GaN FETs. The rectifier circuit also needs to be designed to be in the soft switching operation mode to avoid excess power losses and keeping the high efficiency of the entire system. The targeted input voltage for this converter is in the range of 37 to 57 V_{DC} to support both Power-over-ethernet (PoE) (IEEE 802.3af) and PoE+ (IEEE 802.3at) standards. The PoE powered device can draw power up to 25.5 W according to the IEEE802.at standard or 12.95 W according to IEEE802af [98]. More information about the application and the specification of the circuit can be found in [99], Appendix A-C5.

The converter schematic is shown in figure 5.10. The converter is designed assuming a resistive load. The rectifier circuit is implemented using low forward voltage schottky diodes connected to the load resistance.

Then the input impedance of the rectifier is calculated using equation 5.1 according to [100].

$$R_{in\_rec} = \frac{2 \cdot R_{load}}{\pi^2} \qquad \text{Equ. 5.1}$$

Where R_{load} is the load resistance (50 Ω) – used as a test load.

Then the inverter's loaded quality factor can be calculated using equation 5.2 according to [100].

$$Q_L = \frac{\sqrt{\left(\frac{L}{C}\right)}}{R_{in\_rec}} \qquad \text{Equ. 5.2}$$

Where L is the inductance of the resonant tank, C is the capacitance of the resonant tank, and R_{in_rec} is the input resistance of the rectifier.

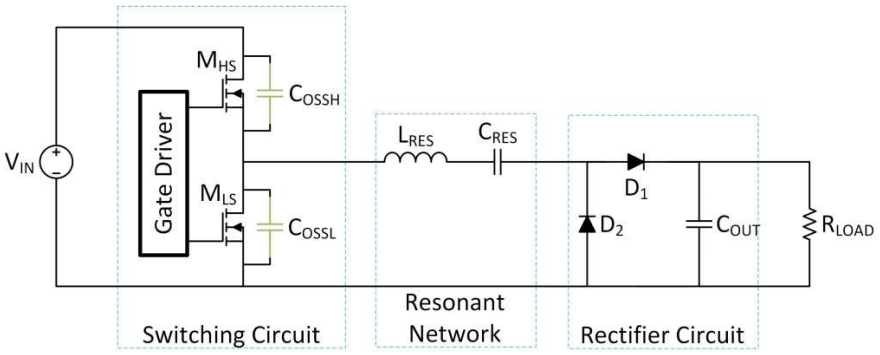


Figure 5.10: Class-DE series resonant DC-DC converter

The total voltage gain (M_V) for the converter can be calculated using equation 5.3 [100]. The voltage gain is then plotted in figure 5.11 for better visualization of the effect of quality factor and switching frequency on the converter's output voltage.

$$M_V = \frac{1}{\sqrt{1 + Q_L^2 \cdot \left(\omega_n - \frac{1}{\omega_n}\right)^2}} \qquad \text{Equ. 5.3}$$

Where ω_n is the normalized switching frequency and Q_L is the inverter loaded quality factor

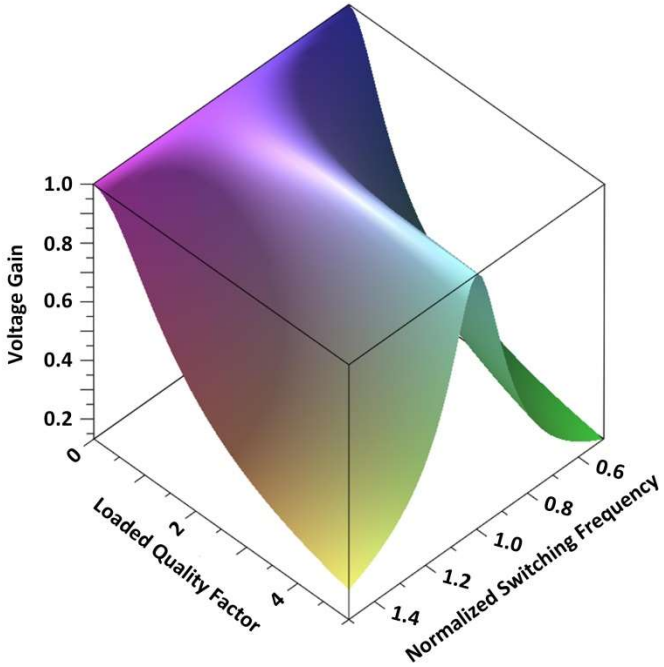


Figure 5.11: Voltage Gain versus Loaded Quality Factor and Normalized Switching frequency

The inverter is designed using EPC8010 [101] gallium nitride FETs from EPC driven by an LM5113 half bridge gate driver from Texas Instruments, a 4.7 nF ceramic capacitor and an AT536RATR49_SZ 491 nH air-core inductor from Coilcraft. The load resistance is set to 50 Ω as a first order approximation to the LED string. A photograph of the converter is shown in figure 5.12.

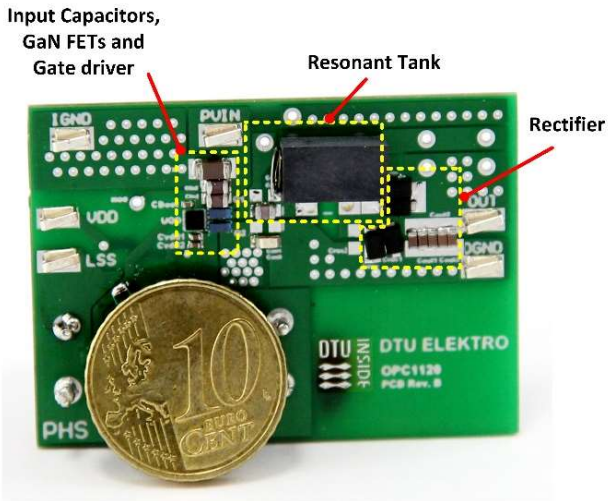
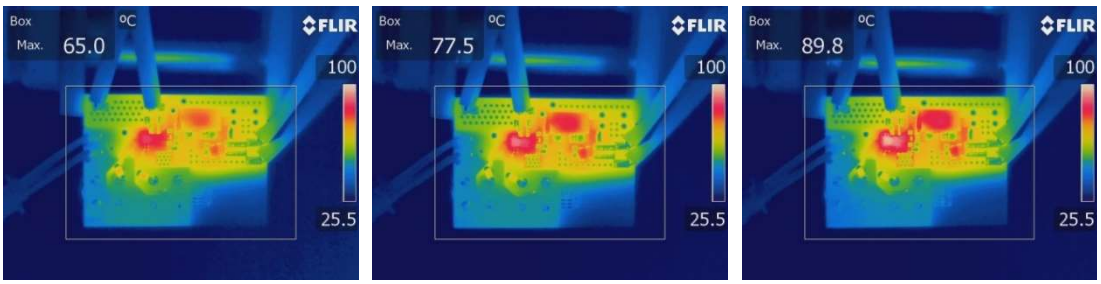


Figure 5.12: A photograph of the HF class-DE series resonant DC-DC converter

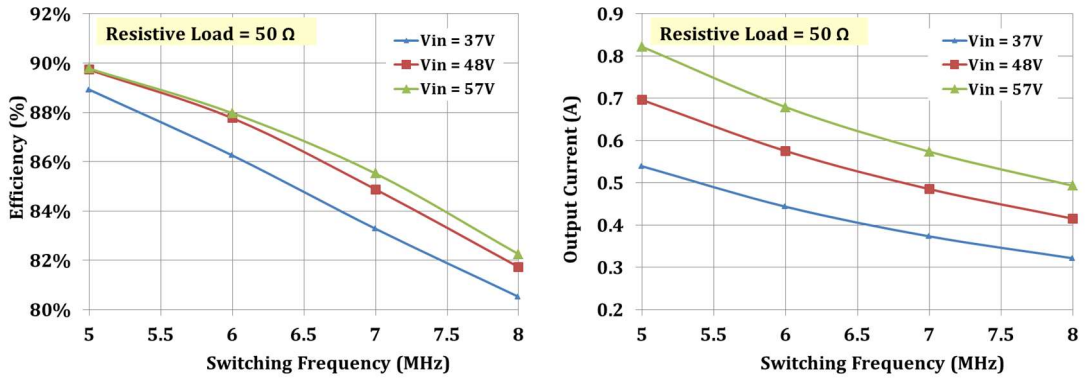
The converter was tested for input voltages between 37 V and 57 V. Thermal photographs at three different input voltages for the converter switching at 6 MHz are shown in figure 5.13. The images show a maximum temperature of 89.8 °C on the gate driver surface.



(a) (b) (c)

Figure 5.13: Thermal images for the HF class-DE series resonant DC-DC converter at three different input voltages.
(a) VIN = 37 V, FSW= 6 MHz
(b) VIN = 48 V, FSW= 6 MHz
(c) VIN = 57 V, FSW= 6 MHz

In terms of efficiency, the converter achieves 88% efficiency converting 57 V input voltage to 34 V output voltage and delivering 23 W to the 50 Ω resistive load while the switching frequency is set to 6 MHz. Efficiency versus switching frequency at three different input voltages is shown in subfigure 5.14a while output current versus switching frequency as a control parameter is shown in subfigure 5.14b.



(a) (b)

Figure 5.14: Measured efficiency and output current for the HF class-DE series resonant DC-DC converter at three different input voltages.
(a) Efficiency versus switching frequency
(b) Output current versus switching frequency

5.2.2 A VHF Class-E Resonant DC-DC Boost Converter

A class-E resonant inverter is built around the custom designed Superjunction MOSFET described in chapter 3. The circuit is designed to operate from an input voltage range of 24-34 V, output voltage of 50 V, and switching frequency of 30 MHz. The Superjunction MOSFET is driven by a self-oscillating gate drive to minimize the gate driver related losses. The converter design follows the procedure given in [57], [59].

A schematic of the converter is shown in figure 5.15. the rectifier is implemented using MBR0560 silicon schottky diodes. The resonant network is formed using 1.2µH ceramic core inductor (LRES) and 100pF C0G ceramic capacitor (CRES). The gate-inductor (LG) is a 100 nH ceramic core inductor. The input inductor L1 is 1 µH.

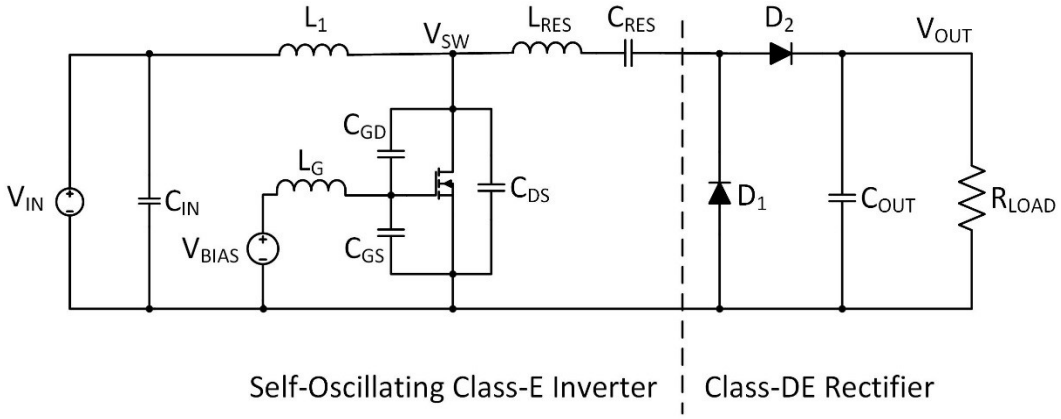


Figure 5.15: Schematic of the self-oscillating class-E DC-DC converter.

A photograph of the prototype is shown in figure 5.16. the Superjunction MOSFET is packaged in a 28 pin 4 mm x 4 mm QFN.

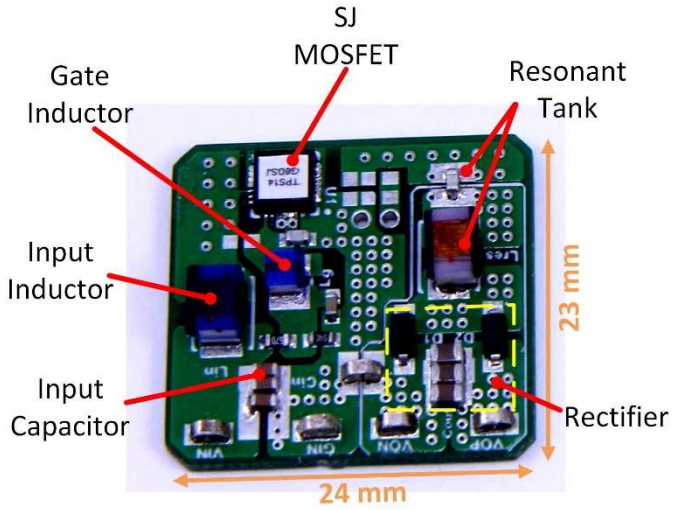
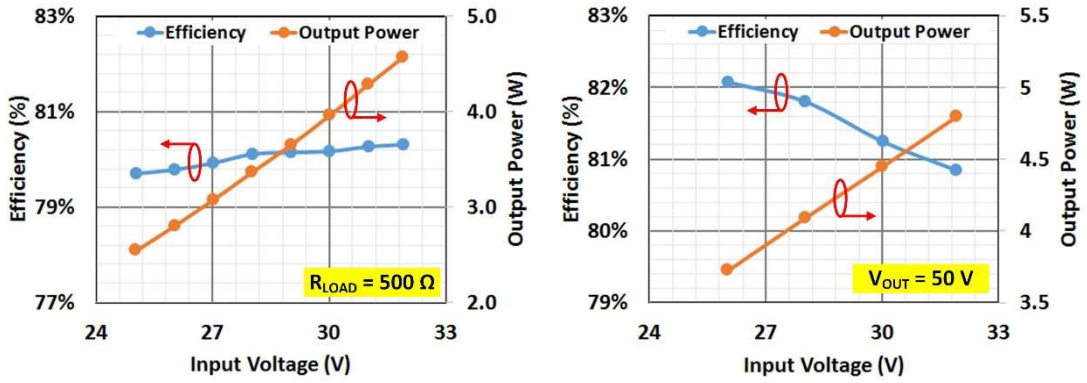


Figure 5.16: Self-Oscillating class-E DC-DC converter using silicon Superjunction MOSFETs

Efficiency and output power as a function of changing the input voltage is measured and reported in figure 5.17 where the converter is tested in two different modes of loading. The first mode -shown in subfigure 5.17a- is constant resistance mode where the resistance is emulated using an electronic load. the voltage conversion ratio is 1.46 on average.

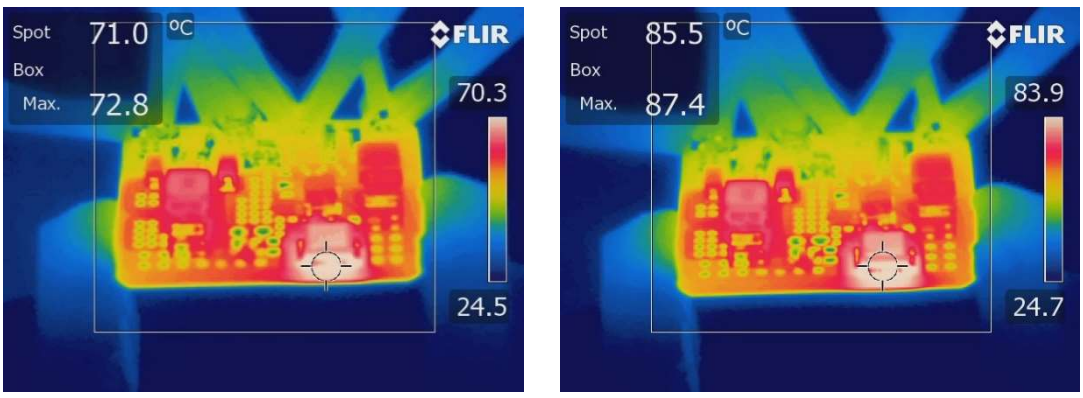
The second mode -shown in subfigure 5.17b- is the constant voltage mode where the output voltage is regulated manually to 50 V. the converter achieved 82 % efficiency when converting 26 V input voltage to 50 V output voltage and delivering 3.7 W to the load.

Thermal images of the converter switching at two different loading conditions is shown in figure 5.18. The highest temperature component is the Superjunction MOSFET. The temperature is peaking at 87.4 ^{o}Cat 32 V input delivering 4.8 W to the load.



(a) (b)

Figure 5.17: Efficiency and output power versus input voltage of the Self-Oscillating class-E DC-DC converter.
(a) Constant resistance load
(b) Constant voltage load



(a) (b)

Figure 5.18: Thermal images of the Self-Oscillating class-E DC-DC converter (no air-flow)
(a) At input voltage of 26 V and output voltage of 50 V delivering 3.73 W to the load
(b) At input voltage of 32 V and output voltage of 50 V delivering 4.8 W to the load

5.2.3 A VHF Class-E Derived boost converter using eGaN FET

A 8.4 V VHF class-E derived boost converter is designed to test DTU manufactured MEMS inductor reported in chapter 4. The selected MEMS inductor to test has 44.6 nH of inductance and a quality factor of 13.3 at 33 MHz. The converter schematic is shown in figure 5.19. the converter consists of two parts.

The first part is a class-D current driven rectifier [100], [102] which is used to drive the load resistance. The rectifier allows DC power flow through D2 to the load and AC power flow through rectification. The diodes used in circuit is silicon schottky diodes (PMEG4010BEA from NEXPERIA).

The second part is a class-E inverter which consists of an input choke (L_1), a GaN FET (M_1), a capacitor (C_{ext}) and finally the inductor under test (L_2). The GaN FET is driven by a logic buffer with an output stage of five inverters connected in parallel.

The frequency is set by an oscillator with a fixed duty cycle of 50 %. L_2 is used as a part of the resonant network, and it also delivers DC current to the load. L_1 has a high inductance and it is mainly carrying DC current so, the AC losses are minimal. L_1 is chosen to be a multi-layer ferrite core inductor. More about the implementation, operation principle, and component selection can be found in [90], Appendix A-J3.

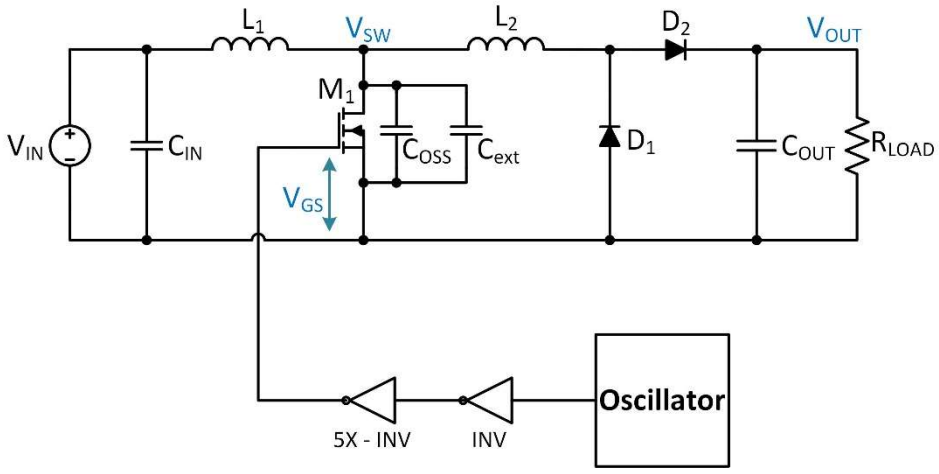
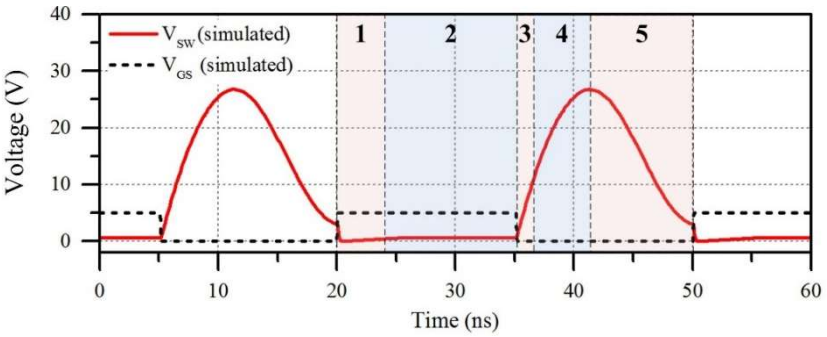


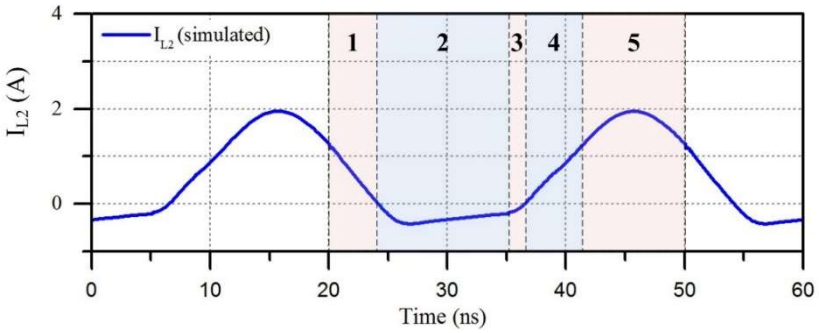
Figure 5.19: A schmatic of class-E derived boost converter

The converter is designed and fine-tuned via SPICE simulations. The input voltage (V_{IN}) is set to be 8.4 V_{DC}. The load resistance (R_{LOAD}) is a fixed 20 Ω resistive load. The simulated waveforms of the switching node (V_{SW}), gate-to-source voltage (V_{GS}), and the inductor current (I_{L2}) are shown in figure 5.20.

The switching node waveform indicates that the converter is operating close to ZVS mode. C_{ext} is tuned externally to achieve ZVS operation since L_2 is fixed at 45 nH. A 180-pF external capacitor (C_{ext}) is optimized to achieve soft switching operation. L_1 is selected to be 1 µH. From the waveform of I_{L2}, the root-mean-square (RMS) inductor current is approximately 1 A with a mean value of 0.56 A. The simulated voltage conversion ratio (V_{OUT}/V_{IN}) is 1.56.



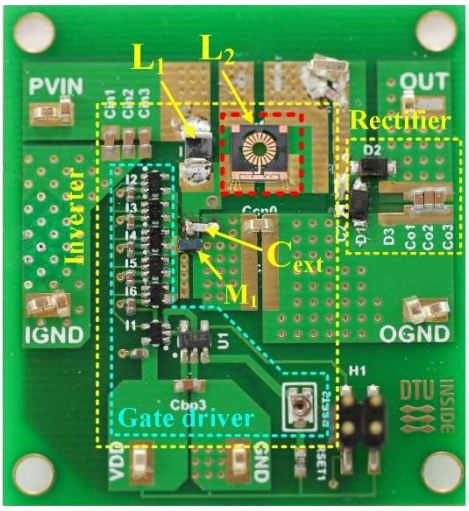
(a)



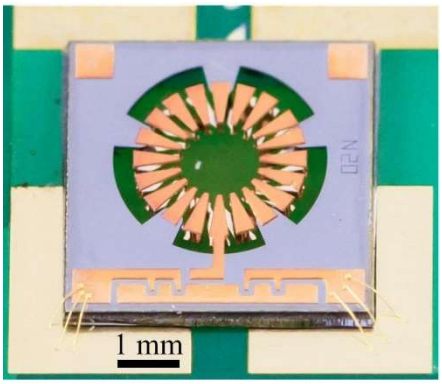
(b)

Figure 5.20: Simulation waveforms of the class-E derived boost converted.
(a) Switching node voltage (V_{SW}) and gate-to-source voltage (V_{GS})of the GaN FET.
(b) Current through the inducotr under test (L_2)

A photograph of the prototype is shown in figure 5.21 where the inductor under test is wire-bonded to the test board after applying an epoxy adhesive underneath the inductor. The total PCB size is 40 mm x 40 mm. The gate driver section is powered externally by a 5 V source.



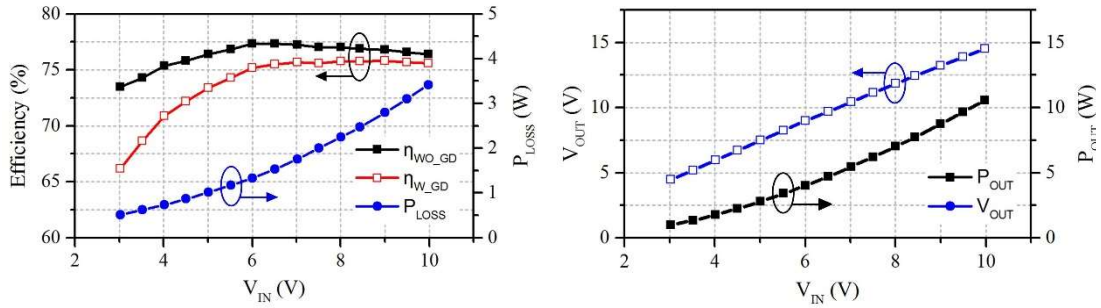
(a)



(b)

Figure 5.21: A photograph of the assembled class-E derived boost converter
(a) a full view of the printed circuit board
(b) a close-up of the inductor showing the bond-wires.

A summary of efficiency and total power loss is shown in figure 5.22a. additionally, output voltage and output power versus input voltage is summarized in subfigure 5.22b. The measured average voltage gain of the converter is 1.48. Efficiency is measured with a sweep of input voltage (V_{IN}) from 3 V to 10 V. the maximum drain efficiency is 77.3% at about 6 V input voltage. The total power loss of the gate driver section is 0.15 W. The maximum power the converter can deliver to the load is approximately 10 W at input voltage is 10 V.



(a) (b)

Figure 5.22: Measured results of the class-E derived boost converter (with air-flow)
(a) Efficiency and total power loss versus input voltage
(b) Output voltage and output power versus input voltage

5.3 Summary

In this chapter, four different topologies were presented. These topologies are categorized to two main types, QSW-ZVS buck converter and resonant power converters. To summarize the advantages and disadvantages of each topology table 5.2 is introduced.

Table 5.2: Comparison between QSW-ZVS Buck and Resonant converters

	QSW-ZVS Buck	Resonant Converters
Advantages	• Low complexity. • PWM control can be used. • Lower inductor value • Ability to switch at HF. • Low components count.	• Soft switching is guaranteed by good design. • Ability to switch at HF and VHF.
Disadvantages	• ZVS is optimized for a single loading condition. • Combined DC and AC inductor current. • Non-overlap control is needed	• Non-overlap control is needed for Class-DE. • Higher components count. • More complex control.

Furthermore, a summary of the topologies and main results are summarized in table 5.3.

Table 5.3: Summary of the prototypes presented in this chapter

Topology ➔		**QSW-ZVS buck**			**Class-E-derived boost**	**Class-DE series resonant**	**Class-E series resonant**
V_{IN}	V	12-24	40-80	12	3-10	37-57	25-32
V_{OUT}	V	5	11.5-14.5	5	--	30	50
P_{OUT}	W	5	12	2.4	10	21	4.8
F_{SW}	MHz	10	5-8	12	33	5-8	28
Power Density	W/cm^3	--	20	--	--	7	--
Efficiency	%	84.7	88.5	72	77	88	82
Gate Driver		Conventional					Self-oscillating
Semiconductors		GaN	GaN	GaN	GaN	GaN	Custom Si SJ-MOSFET
Magnetics		Custom PCB-Spiral	Ceramic-core	Custom NiZn Core	Custom Air-core	Air-core	Ceramic-core

Chapter 6

Integration and packaging

The advances in power semiconductor devices, passive components, and the converter topologies create more opportunities to achieve higher power densities and seeking the goal of PwrSoC. Advanced assembly and packaging methods play a vital role to achieve the needed performance and the smallest sizes possible. Many manufactures nowadays provide their products on a wafer level, wafer level packaged die forms, or flip-chip in package form. This shift to advanced packaging in semiconductor components not only enabled smaller power supplies but also achieving efficient operation.

Efficiency is a key parameter in any power supply, but it is always important to look at absolute numbers of power losses as they are dictating the self-heating of the individual components.

In this chapter, three different technologies are visited to achieve closer proximity of the components in a power supply unit, embedding component in substrates, and finally molding of power stages and its effects on power supply performance. Section 6.1 discusses chip-on-board (CoB) assembly of power FETs as an alternative of conventional packaging. Section 6.2 discusses a power supply integration method on silicon interposers with embedded magnetics. A thermally-enhanced encapsulation of power-stage-in-package is studied in section 6.3.

6.1 Chip-on-Board Assembly of a Superjunction MOSFET

Chip-on-board is an assembly technique where a semiconductor die is attached directly to the application substrate (e.g. a PCB) the electrical connections are established via bond-wires. The custom-layout designed lateral Superjunction MOSFET described in chapter 3 is used in the Class-E VHF converter which is realized, tested and reported in chapter 5. A modification to the PCB layout and surface finish is incorporated to allow gold wire-bonding. Figure 6.1 shows two variants of the converter. The Superjunction MOSFET die is attached to the PCB using a non-conductive epoxy adhesive and manually wire-bonded to the PCB using 25 µm gold wires.

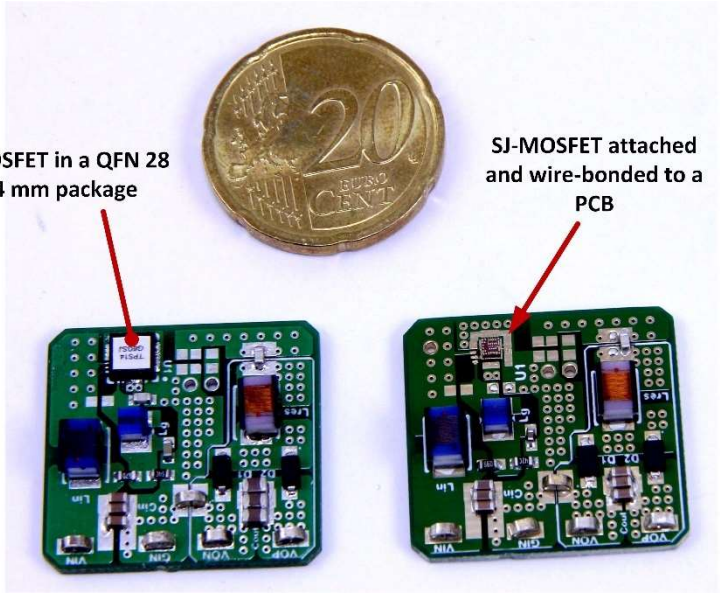
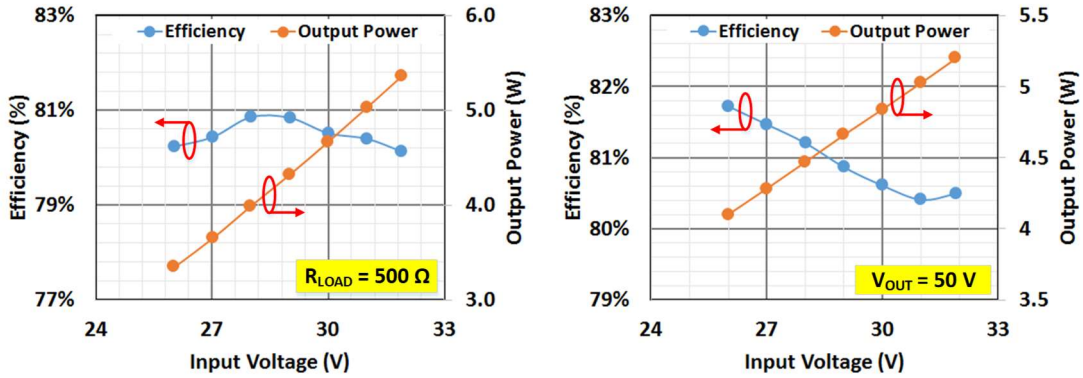


Figure 6.1: Two variants of VHF Class-E DC-DC converter together with a 20 € cent coin.

The converter is tested electrically, and the results are summarized in figure 6.2. Efficiency and output power as a function of the input voltage is measured and reported in figure 6.2 where the converter is tested in two different modes of loading. The first loading mode (shown in subfigure 6.2a) is constant resistance mode where the resistance is emulated using an electronic load and set to 500 Ω. the voltage conversion ratio is 1.6 on average. The higher voltage conversion ratio is due to the slightly higher bias voltage for the self-oscillating gate driver.

The second loading mode (shown in subfigure 6.2b) is the constant voltage mode where the output voltage is regulated manually to 50 V by varying the load resistance. The converter achieved 81.7 % efficiency when converting 26 V input voltage to 50 V output voltage and delivering 4.1 W to the load.

Although is it difficult to accurately measure the temperature of the MOSFET due to the reflection coefficient of the silicon surface. An indication of the temperature can be noticed from the surroundings of the device. Thermal image of the converter is shown in figure 6.3. where the converter input is set to 30 V and the output voltage is 50 V delivering 4.85 W to the load. The highest temperature component is the Superjunction MOSFET.



(a) (b)

Figure 6.2: Efficiency and output power versus input voltage of the Self-Oscillating class-E DC-DC converter.
(a) Constant resistance load
(b) Constant voltage load

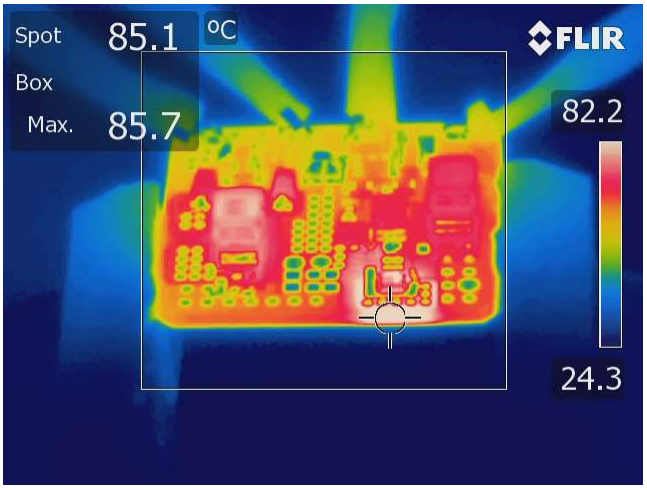


Figure 6.3: A thermal image of the Self-Oscillating class-E DC-DC converter with a CoB MOSFET.

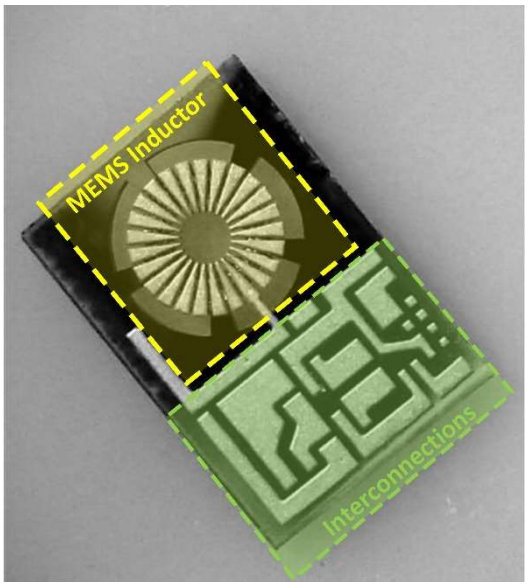
6.2 Three-Dimensional Silicon-Passive-Interposer-Based PSiP

Three-dimensional magnetic structures can be embedded in silicon substrates is demonstrated in chapter 4. Thick metal deposition in both sides of a semiconductor wafer enabled the construction of interconnection to stacked-devices soldered on pad openings on the surface of the substrate.

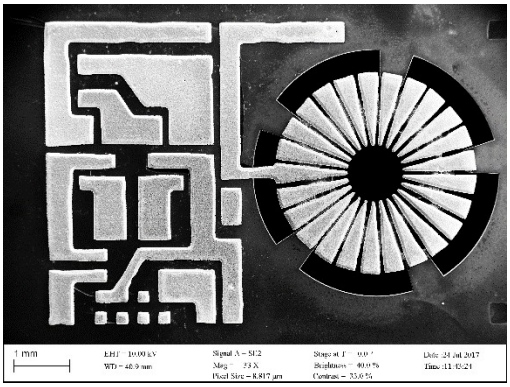
A silicon interposer that has dimensions of 4.5 x 8 x 0.28 mm is designed and manufactured in silicon wafers using a CMOS compatible process developed at DTU national center for micro- and nanofabrication (DTU Danchip). A QSW-ZVS buck topology is selected for demonstration.

Figure 6.4 shows the manufactured interposer after dicing out of the wafer. The die has two regions. The first region is shaded in light green color where the interconnection of the circuit is implemented using thick copper after deposition of a passivation layer. The area may

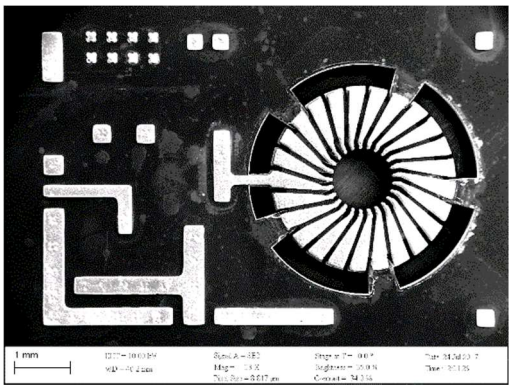
contain active devices embedded in the silicon substrate. The second region is shaded in yellow is where the 3D-magnetic structures is realized.



(a)



(b)



(c)

Figure 6.4: A Silicon interposer with embedded 3D magnetic structure.
(a) An optical photograph of the interposer top side
(b) An X-ray scan of the interposer top surface
(c) An X-ray scan of the interposer bottom surface

The power stage is designed to operate at high switching frequency and up to the VHF spectrum. The prototype integrates two 40 V GaN FETs driven by a high frequency half bridge gate driver, and an in-silicon inductor, in addition to input and output capacitors.

The in-silicon inductor could be fabricated with a nonmagnetic-core (e.g. air core, thermal-conductive polymers), or integrated magnetic core (e.g. composite core by screen-printing, electroplated solid or laminated core). All the mounted components are commercially available. Figure 6.5 shows the device schematic with all internal components together with a photograph of the assembled converter.

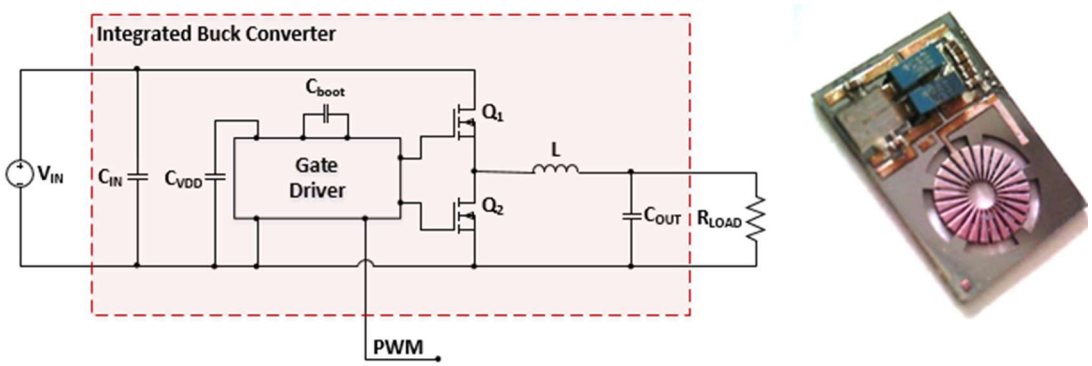


Figure 6.5: A simplified schematic and photograph of the PSiP

The components which is used in the realization of this prototype is summarized in table 6.1. The converter is mounted on the 40 mm x 40 mm test board has an oscillator which allows generating a controlled frequency square-wave signal with a 50% duty-cycle. It also allows injecting a signal from a function generator with the desired duty cycle.

Table 6.1: The PSiP internal components

Symbol	Part Number	QTY	Description
Q_1, Q_2	EPC8004	2	40 V eGaN FET
Gate Driver	PE29100	1	High-Speed gate driver
L	*Custom Design*	1	47.5 nH air-core toroidal inductor
C_{OUT}	GRM033C71C104ME14D	4	0.1µF, 0201, 16V, X7S Ceramic Cap.
C_{IN}	GRM033C71C104ME14D	7	0.1µF, 0201, 16V, X7S Ceramic Cap.
C_{BOOT}, C_{VDD}	GRM033C71C104ME14D	2	0.1µF, 0201, 16V, X7S Ceramic Cap.

The prototypes are manually assembled using two types of solder pastes with different melting temperatures. These two solder pastes are $Sn_{96.5}Ag_3Cu_{0.5}$ with melting temperature of 217 °C (paste 1) and $Sn_{63}Pb_{37}$ with melting temperature of 187 °C (paste 2). Both solder pastes have type 5 particles (15-25 µm). Solder-paste 1 is used to assemble the interposer components by dispensing the solder using a fine needle. Then, the interposer is optically and electrical checked. Solder-paste 2 is used to assemble all the components on the board including the pre-assembled interposer. The assembled test board with a zoomed in view of the interposer is shown in figure 6.6.

The converter is designed, simulated using LT-Spice software, and then experimentally tested. The simulated and measured waveforms of the converter are presented in figure 6.7. Simulation waveforms for the converter's switching node and inductor current with an input voltage of 5 V and an output voltage of 3.3 V with a load current of 270 mA at switching frequency of 21 MHz are shown in subfigure 6.7a. Measured switching node voltage and the low side switch gate-to-source voltage are presented in subfigure 6.7b under the same testing conditions.

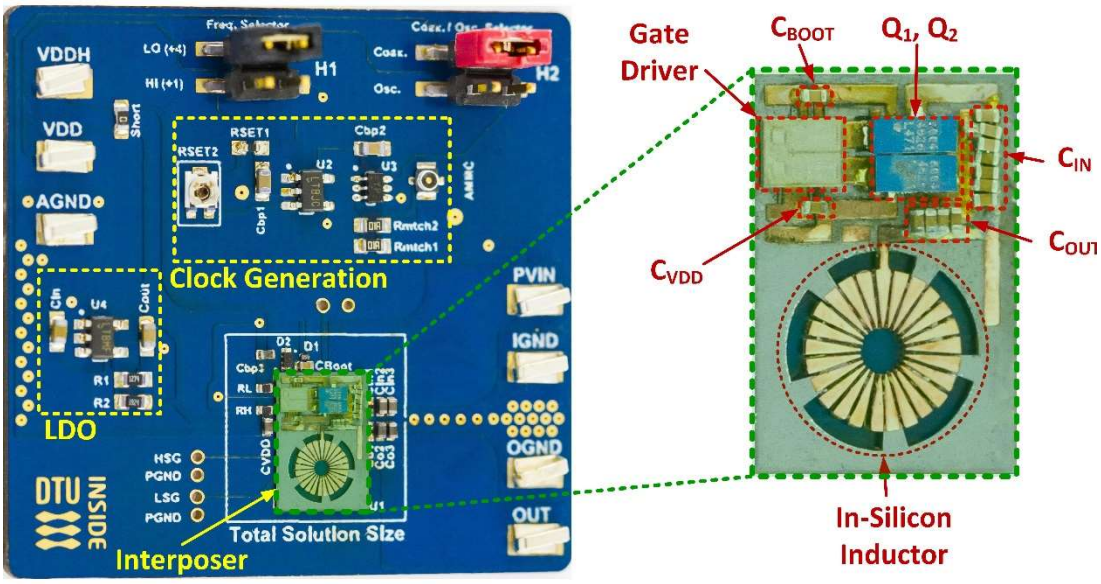


Figure 6.6: The test board for the PSiP together with a zoomed in photograph of PSiP

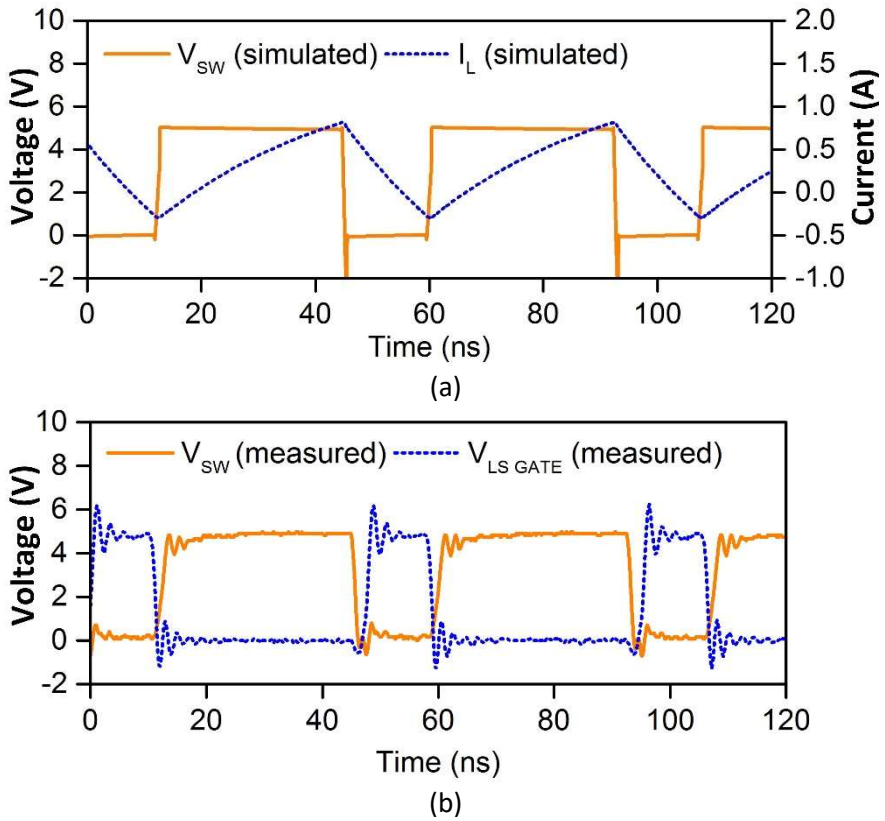
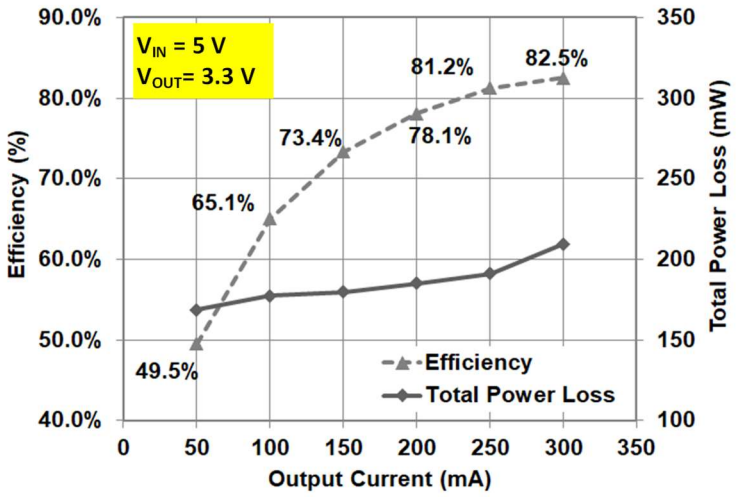


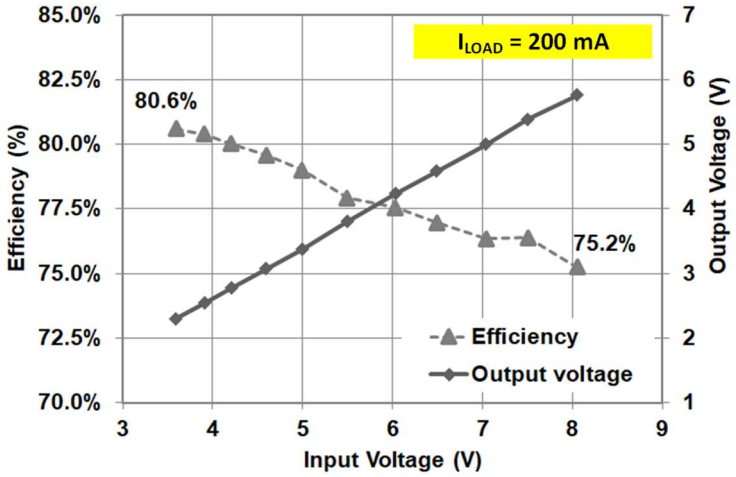
Figure 6.7: Simulated and measured waveforms of the PSiP
(a) Simulated switching node voltage and inductor current waveforms
(b) Measured Switching node voltage and low side gate-to-source voltage waveforms

The converter is test with input voltage range of 3 V to 8 V and the switching frequency is set to 21 MHz. Efficiency and total power loss of the converter with input voltage of 5 V and output voltage of 3.3 V at different loads are shown in figure 6.8. The maximum efficiency achieved is 82.5% at load of 300 mA. Thermal images of the converter (figure 6.9) show that

the gate driver is the component with the highest temperature of 55 °C. It is possible to fill the core of the inductor with a magnetic material to increase the inductance value. Then by reducing the switching frequency, it is expected to gain a few efficiency points and enhance the input voltage range and achieve higher output power of the converter without increasing the volume or the footprint of the converter. This concept is tested in a discrete converter using a similar magnetic core inductor. More information about this experiment is presented in Appendix A-J1.

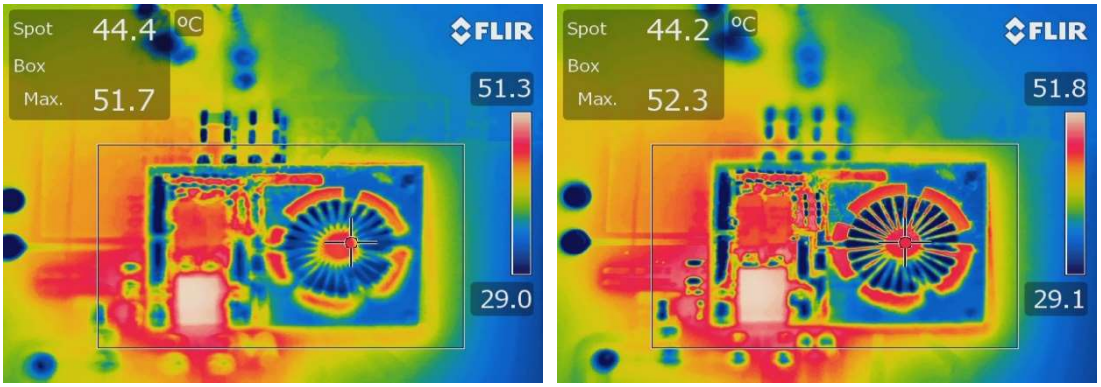


(a)



(b)

Figure 6.8: Measured Efficiency curves of the PSiP
(a) Efficiency and total power loss versus load current for V_{IN} = 5 V, V_{OUT} = 3.3 V
(b) Efficiency and output voltage versus input voltage at fixed load current of 200 mA and fixed duty cycle of 65%



(a) (b)

Figure 6.9: Thermal photographs of the PSiP switching at 21 MHz, V_{IN} = 5 V, V_{OUT} = 3.3 V
(a) No-load current
(b) 270 mA loading condition

6.3 Thermally-Enhanced Encapsulation of GaN-Based Module

In many power electronic circuits, hot-spots may exist especially when very small footprint components are used. Establishing a thermal conduction path between the hot electrical components and the cold electrical components will lead to homogeneous temperature profile and lower peaks of temperatures. Eventually, the electronics circuit will have better performance.

One can design an electrical component with bigger size to avoid self-heating. Hence, this approach contradicts with the miniaturization trend in modern power electronic systems. Another example of power electronics cooling techniques is using heat sinks or heat pipes to transfer the heat from the hot electronic part to wider and cooler areas in the system. Using such an approach will increase the volume and the weight of module significantly.

To tackle this problem in small area and volume power supplies two approaches are investigated in this work. The first approach is to use substrate materials with high-thermal conductivity such as Alumina, AlN substrates, metal-core substrate, or even silicon interposers. The second approach is power converter molding using high thermal conductivity material. From the study determined in chapter 2, most commercial products are molded using an epoxy material loaded with silica particle to enhance the coefficient of thermal expansion (CTE) and other thermos-mechanical properties of the molding compound. If higher thermal conductivity compound is needed, ceramic particles can be added.

In this section, thermal simulations using SOLIDWORKS software are used to investigate the possibilities to achieve better thermal behavior of the GaN-based module described in chapter 5.

6.3.1 Modelling of GaN-based Modules in SOLIDWORKS CAD Environment

A simplified model of the PCB is constructed in SOLIDWORKS environment. The 0.6 mm finished thickness two-layer PCB model is presented in figure 6.10. The materials are defined to match the manufactured PCB substrate for the module. All the components in the module are modelled, however, the simulation time increased dramatically. Therefore, a more simplified model is built using the components where most of the power losses exist. Based on the calculations and simulations, the ceramic-core inductor power-loss is set to 1 W, the high-side GaN FET power loss is set to 0.2 W and the low-side GaN FET is set to 0.3 W. The model used for simulations is shown in Figure 6.11.

Steady-state simulations of the model are carried out and the results are presented in figure 6.12a. Simulation results show agreement with the temperature signature of the module when it is tested experimentally. Figure 6.12b shows a thermal photograph of the module operating at input voltage of 40 V, output voltage of 13.5 V, and load current of 900 mA.

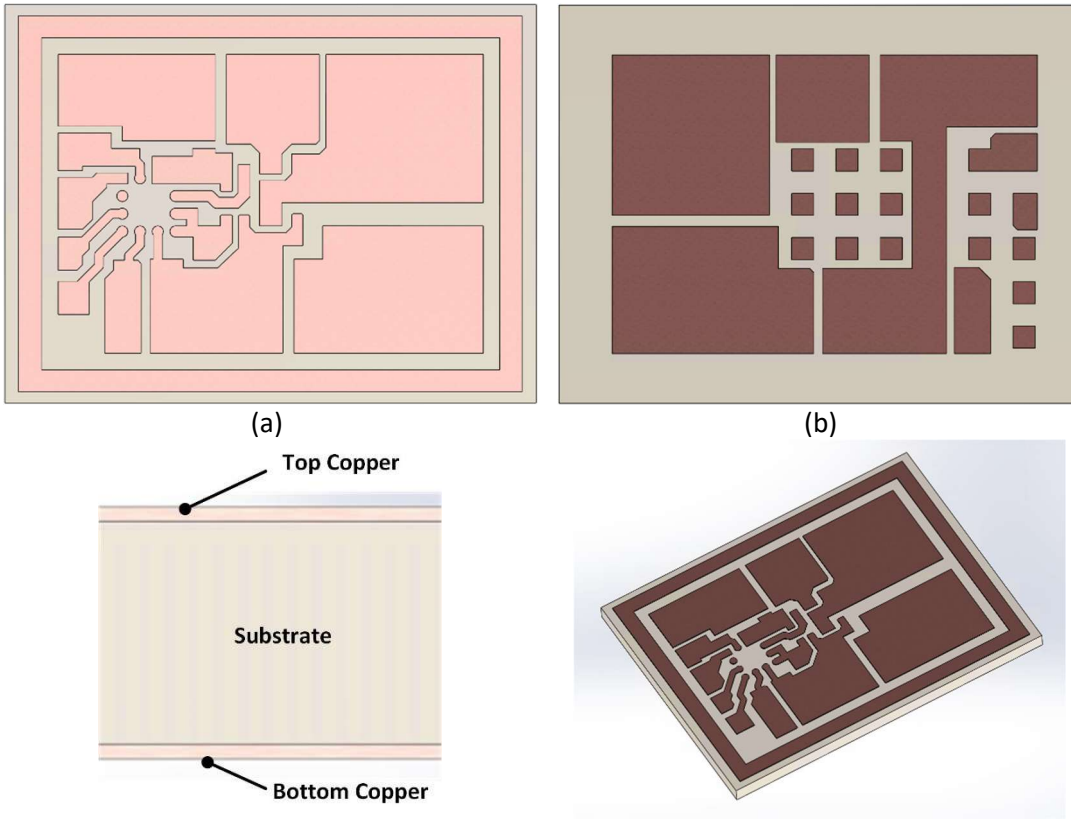


Figure 6.10: Model for the GaN Module Substrate in SOLIDWORKS
(a) Top-view (b) Bottom-view
(c) Cross-sectional view (d) Prospective view

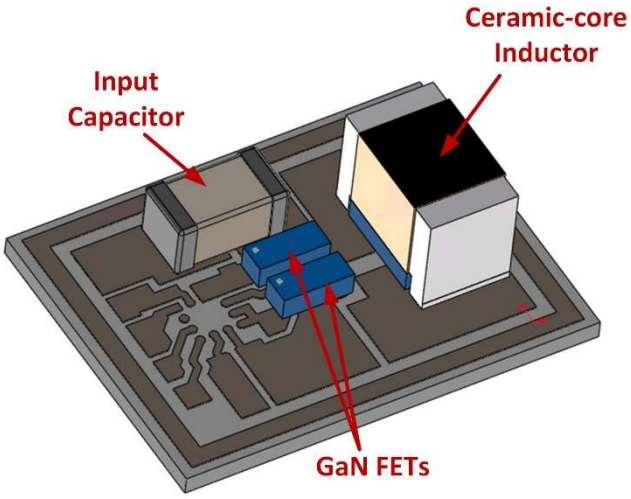
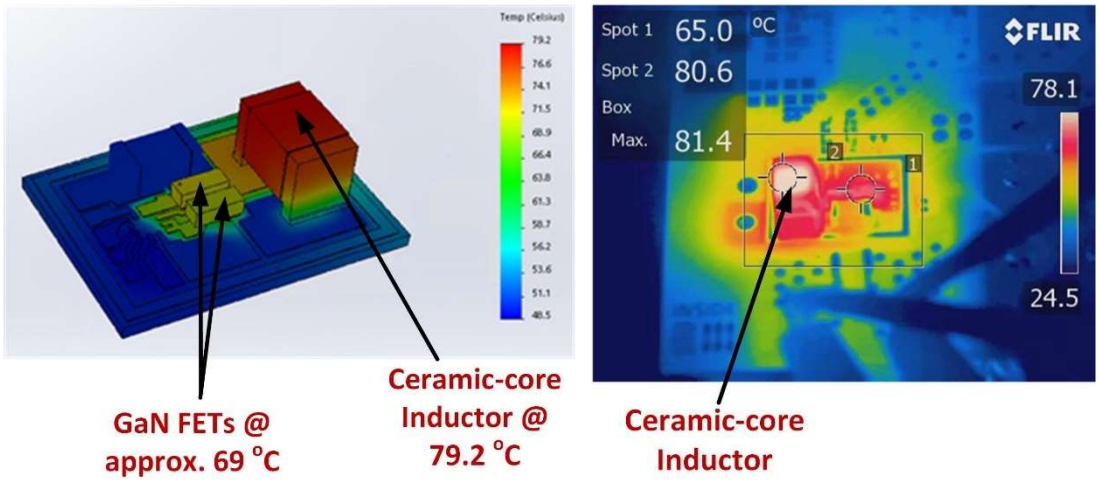


Figure 6.11: Perspective view of the GaN-module simulation model in SOLIDWORKS.



(a) (b)

Figure 6.12: Thermal simulations and experimental results of the GaN-module under steady state condition

(a) Steady-state thermal simulations results

(b) Steady-state thermal photograph

6.3.2 Effect of high-thermal-conductivity substrate materials

Ceramic substrates are used in circuits where thermal conductivity of the substrate is crucial. It is widely used in automotive applications and high-power LED modules. There is a variety of ceramic substrate materials commercially available [103]. The most widely used materials are AL_2O_3, Si_3N_4, AlN, and BeO. A summary of thermal conductivity of ceramic substrates compared with a standard FR4 substrate is presented in table 6.2.

Table 6.2: Examples of PCB substrates

	Substrate Material	Thermal conductivity (W/m-K)	Dielectric Constant	Notes
Ceramic	Alumina (Al_2O_3)	24	9.8-10	Cheaper
	Aluminum Nitride (AIN)	170	9	Expensive
	Beryllia (BeO)	209-330	6.1-7.5	Toxic
	Silicon nitride (Si_3Ni_4)	90	7.5	-
	ZrO_2 doped Alumina (HPS)	26	No-data	-
FR4	RO4003C (From Rogers Corp.)	0.71	3.38	High-Frequency
	FR408 (isola group)	0.4	3.69	High-Tg
	DE104 (isola group)	0.36	4.46	Standard FR4

The effect of substrate material on components temperatures is simulated using an Alumina substrate (fixing the all other design parameters like copper thickness and clearance). Alumina substrate material was chosen due to its availability and lower cost. The simulation results, presented in figure 6.12, show a significant drop of all components temperatures. For example, the ceramic core inductor peak temperature dropped by more than 12 °C from 79.2 °C to 67.1 °C.

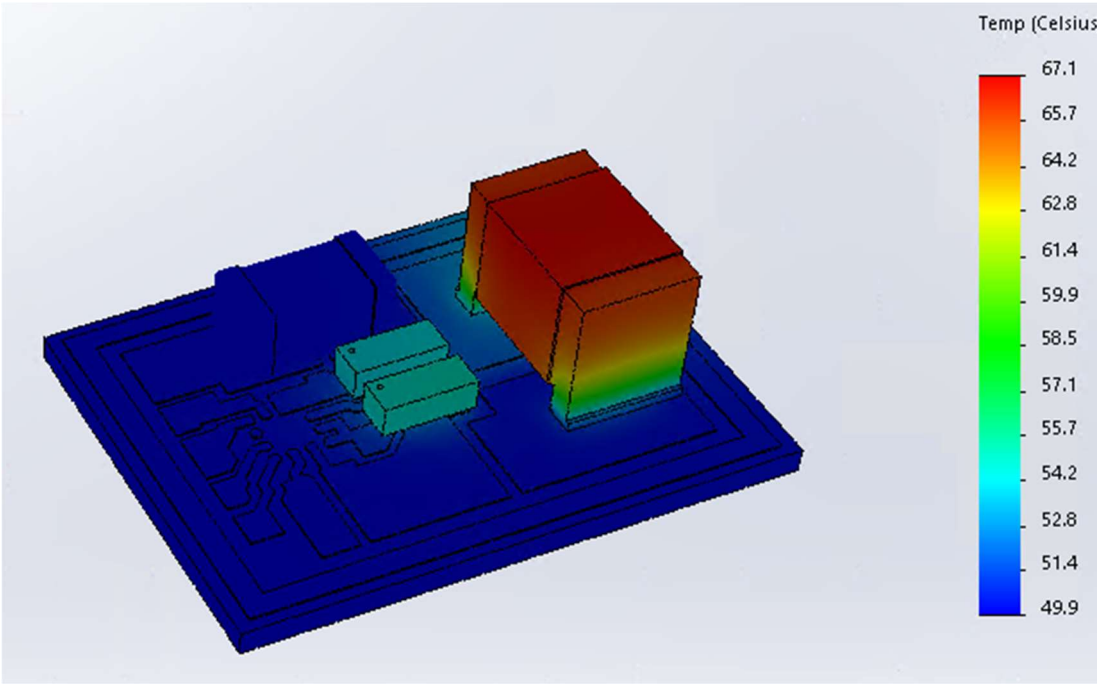


Figure 6.12: Simulation results of the GaN-Based module using an alumina substrate

6.3.3 Effect of encapsulation using a variety of materials

Many power modules are sold in an encapsulated form. To achieve better thermal characteristics of the module, high thermal conductivity epoxy-melding-compounds (EMCs) are used for the encapsulation process. Standard EMCs for semiconductors have a thermal conductivity around 0.9 W/m.K [104]. A High thermal conductivity EMC with a thermal conductivity of 3.4 W/m.K [105] is studied by simulations. Simulation results of the FR4 based GaN module are shown in figure 6.13. The highest temperature is 61.8 °C which is 17 °C temperature drop of the inductor temperature. An EMC material with higher thermal conductivity of 5 W/m.K is used for encapsulation of the GaN-Module with an FR-4 substrate. The simulated peak temperature is dropped even more to 60 °C, or approximately 19 °C drop from the FR4-based module without encapsulation.

Prototypes were encapsulated at Fraunhofer Institute for Reliability and Micro-integration (Fraunhofer IZM). A photograph of multiple encapsulated modules is shown in figure 6.14.

6.3.4 Initial experimental evaluation of the effect of encapsulation

An initial test is carried out to determine the effect of encapsulation using the high thermal conductivity material. Two thin-wires are used to establish an electrical connection to the inductor inside the module from the pads on the bottom side of the FR4 substrate. These two wires are used to apply a DC current through the inductor. This procedure is to mimic the power loss in the inductor as if it is operating in a switch-mode power supply. The same procedure is done in a module substrate without encapsulation. The modules where not mounted on the test PCB. The DC power loss in the two inductors is set to an equal value of 920 mW which was enough to result in rising the temperature of the inductor with no encapsulation to approximately 150 °C. On the other hand, approximately 90°C is observed on the surface of the encapsulated module in a steady state condition. A thermal photograph showing the two modules side-by-side is presented in figure 6.15.

6.4 Summary

In this chapter three different topic were discuss related to packaging and integration of power converters. The first topic is CoB integration of semiconductor power devices to get rid of the packaging limitation. The power device mounted on the PCB and electrically connected to the circuit using 25 µm gold wires. The converter shows normal behaviour without observing any drawbacks. Alternatively, Flip-chip-on-board mounting could be also used to shrink the footprint reserved for wire-bonding and results in low parasitic inductances for the connections.

The second topic is PSiP integration using 3D passive interposer. The interposer is designed, manufactured, and tested and operated at 21 MHz and successfully delivered up to 1.15 W to the load. The input voltage range of the current design is limited to 8.5V. the interconnection part of the interposer is used for stacking GaN FETs, gate driver, and Input/output capacitors. This PSiP is benefiting from the high thermal conductivity of the silicon substrate and low profile of the converter.

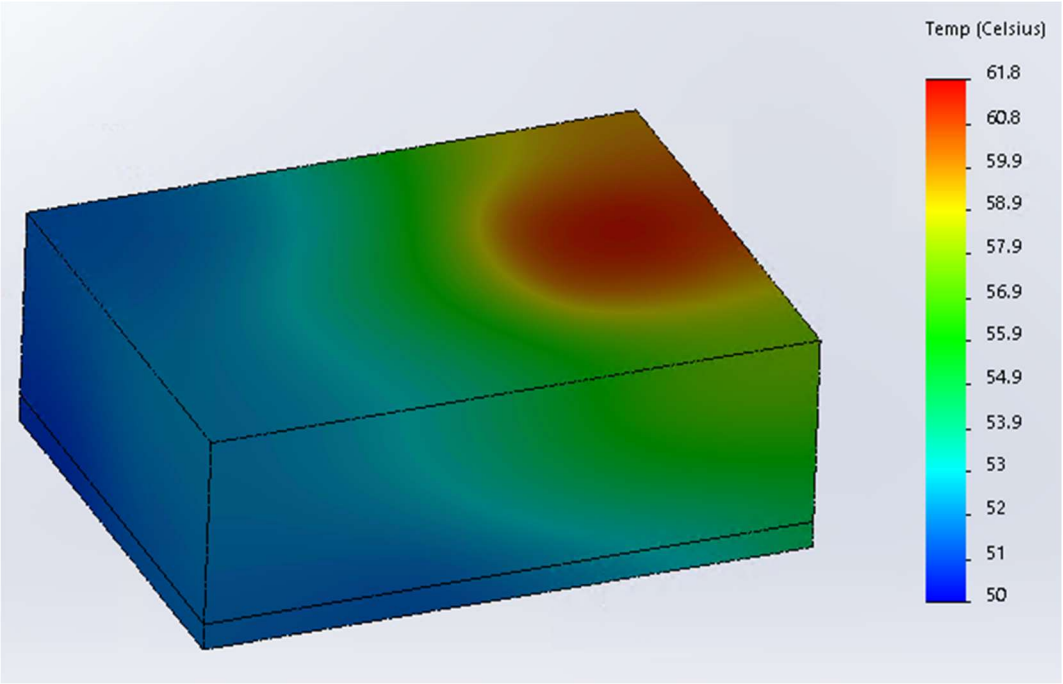


Figure 6.13: Simulation results of the GaN-based module using an FR4 substrate and a high thermal conductivity encapsulation.

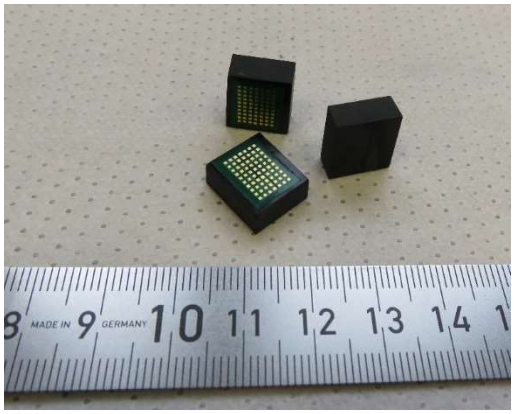


Figure 6.14: Multiple encapsulated GaN modules

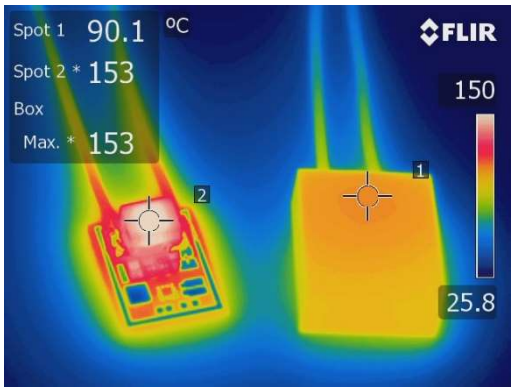


Figure 6.15: Thermal performance of GaN modules before and after encapsulation

The input voltage range, and power density can be extended to higher voltages by adding a magnetic material into the air-core.

Finally, the third topic is describing a method of encapsulating power modules to achieve better thermal performance by alternative substrate and encapsulation methods. Preliminary testing results of the encapsulated module show enhanced thermal performance compared to the module with no encapsulation. This enhancement can be invested in extending the output power of the module or targeting other applications where high ambient temperatures operation is needed. Encapsulation is a standard process. Hence, it suitable for mass production.

Chapter 7

Summary, Conclusion, and Future Work

This chapter includes a summary for the presented work across the thesis, a conclusion based on the research findings, in addition to the future work. Section 7.1 overviews a summary for selected prototypes implemented in the PhD work. The conclusion section 7.2 discusses the most important design considerations based on the results of the conducted work. Eventually, section 7.3 describes the current work taking-place on several implemented prototypes, as well as the work that is suggested for the near future towards more miniaturized power converters.

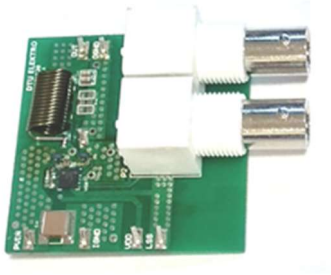
7.1 Summary of prototypes

Selected prototypes and chips designed during the PhD studies are presented in figure 7.1. Some of the prototypes are referred-to in the previous chapters of the thesis. As shown in the figure, the work included the design, implementation and testing of various types of power converters, which include PWM and resonant topologies, HF and VHF operation, discrete and integrated implementations, different inductor structures and integration techniques, in addition to different test boards as well as a characterization board for power semiconductor switches.

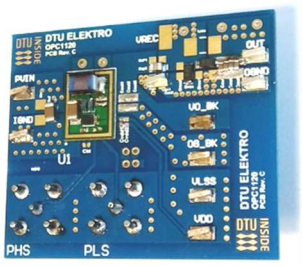
7.2 Conclusion

Energy storage elements are dominating the size and weight of power supplies. This thesis represents a study on technologies targeting the miniaturization of power supply units. The results of this study are summarized in the following points:

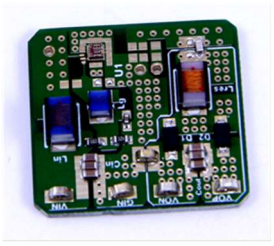
- 150-µm-thick two-layer spiral inductors are designed and utilized in 10 MHz buck converters, showing promising performance. A 5 W converter achieved 84.7% peak efficiency converting 12 V to 5 V and 78% efficiency converting 24 V to 5 V.
- Four types of MEMS inductors were tested in resonant converters and QSW-ZVS buck converters configurations. These four types are air-core, Si-core, NiZn-core, and Novel-core inductors. Two examples of these converters are:
  - A resonant class-E-derived boost converter using air-core toroidal inductor-in-silicon. The converter is switching at 33 MHz. An efficiency of 77% is achieved converting 8.4 V to 12.4 V. The maximum output power delivered to the load is approximately 10 W.
  - A 12 MHz QSW-ZVS buck converter using NiZn-powder-core achieved a peak efficiency of 72% converting 12 V to 5 V. The converter achieved a maximum output power of 2.4 W.
- Four different topologies are studied, designed, implemented, and lab tested through multiple prototypes. These topologies are the QSW-ZVS buck converter, Class-DE series-resonant converter, VHF class-E series-resonant converter, and VHF class-E-derived boost converter. A comparison between these topologies is summarized in section 5.3.
- Three integration and packaging techniques are presented in this thesis. These techniques include:
  - A chip-on-board approach, which is investigated and showed a minimal effect on the operation and efficiency of a VHF class-E converter. The converter achieved 81.7% efficiency when converting 26 V to 50 V and delivering 4.1 W to the load.
  - An interposer-based PSiP, achieving 83% efficiency in a buck converter configuration, where the converter is tested up to 8.5 V input voltage, with the output voltage being set to 3.3 V, and delivering an output power of 1.15 W.
  - Power modules encapsulation using a high-thermal-conductivity material. Although the converter was not fully tested, initial results show the superiority of the encapsulated module, with 63°C reduction in steady-state operation temperature.



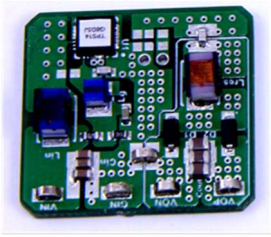
Buck converter stage



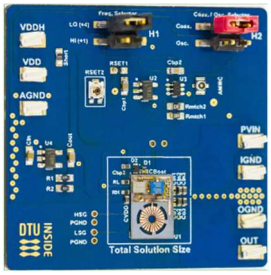
Module test-board



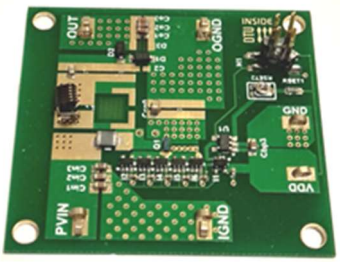
CoB VHF class-E DC-DC



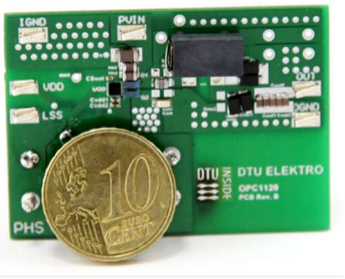
VHF class-E DC-DC



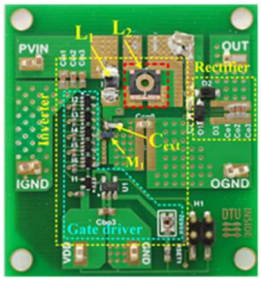
Interposer test-board



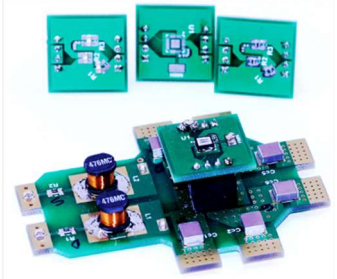
100 MHz class-E DC-DC



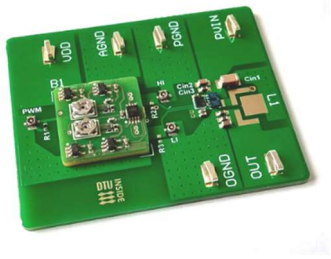
Class-DE DC-DC



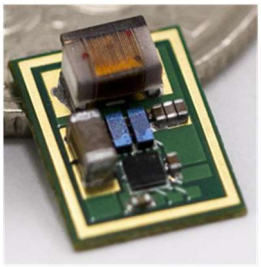
Class-E derived DC-DC



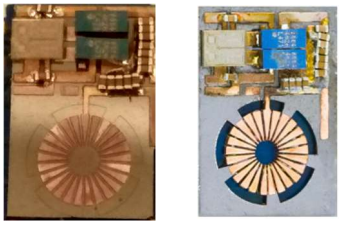
Transistors small-signal characterization board



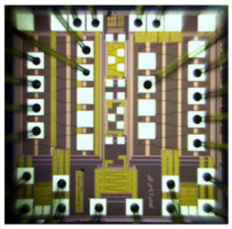
Buck converter for MEMs inductors



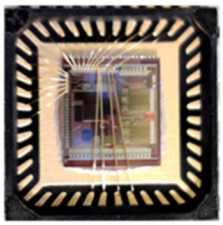
GaN power-stage



Interposers with integrated Si-Core / air-core inductors



Dual 140 V Superjunction MOSFETs chip



Adaptive-deadtime controller chip

Figure 7.1: Overview of selected prototypes designed during the PhD period.

From the conducted work and the results of the implemented prototypes, several design considerations are listed below:

- The emerging gallium nitride power devices technology has shown promising performance compared to the best in-class silicon devices in smaller sizes. However, the reliability of GaN devices is still an open question. It is noted that all the damaged or degraded GaN FETs resulted from the gate side through excessive ringing.
- In half-bridge topologies (including buck converter), the high drain-to-source voltage slew rate causes degradation of the FETs and damages in some cases. Accordingly, the gates parasitic inductances must be minimized, and selecting the right gate driver is vital to avoid this situation.
- Custom design of MOSFET layout for a specific application is beneficial and results in efficiency enhancements.
- MOSFET capacitances must be measured to achieve better designs, especially for soft-switching high-frequency converters. The measurements can be carried out using a special setup as described in Chapter 3 or using a commercial semiconductor characterization equipment, such as the B1505A Power Device Analyzer / Curve Tracer from Keysight.

7.3 Future Work

Many aspects of improvement can be pursued for more enhanced integration towards even smaller power converters with high efficiency. The aspects include, but are not limited to, the following:

- The power semiconductor devices characterization setup can be enhanced and upgraded to support higher voltage devices up to 650 V. This setup has the potential to enable the characterization of power semiconductor devices in a controlled temperature and humidity chamber to study their effects on the device capacitances.
- For magnetics, the spiral inductor designs have the potential for improvement with the addition of two layers of magnetic materials. This work has already started. Subfigure 8.2a shows a spiral inductor sandwiched by two magnetic layers, and planned for testing in an 80 V class-DE DC-DC converter. Additionally, the magnetic-material encapsulation of discrete air-core inductors shows promising initial results. It is expected to test these inductors in high-frequency DC-DC converters and compare the performance to previous designs. Subfigure 8.2b shows one of the encapsulated inductors.

(a) (b)

Figure 7.2: Future work related to magnetics
(a) Sandwiching spiral inductors by magnetic layers.
(b) Magnetic encapsulation of air-core solenoid inductor

- During my external research stay at IMEC, Belgium, I had the chance to get more insight into the GaN devices technology and manufacturing. Two prototypes were designed during my stay. Figure 7.3 presents a low power VHF class-E DC-DC converter using GaNFETs. Testing this converter is part of the future work.

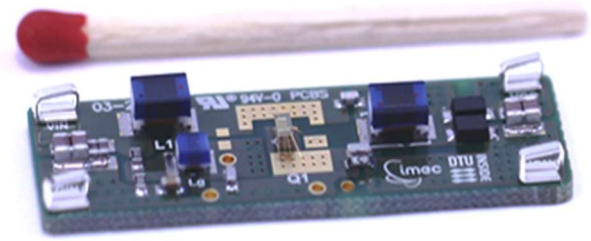


Figure 7.3: A Class-E VHF converter using GaNFETs manufactured by IMEC.

- For PSiP and PwrSoC integration, one of the future directions for low-voltage and medium-voltage converters is the enhancement of the existing interposer technology by magnetic material deposition and realizing embedded capacitors. Another direction in this domain is developing and fabricating active-passive (hybrid) interposers as reported in appendix A-P1.
- The concept of realizing active-passive interposers is shown in figure 7.4, where the active circuits are manufactured and delivered in a wafer form, followed by the embedding of the MEMS inductors and capacitors into the substrate by the process developed at the Technical University of Denmark.

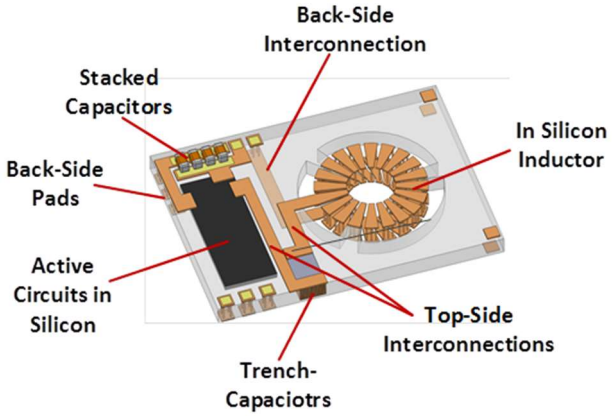


Figure 7.4: The PwrSoC concept reported in Appendix A-P1.

- As stable and precise supply voltage/current is a must in most of the electronic systems, various control circuits were reviewed and investigated. The relevant control techniques for two of the most used converter are discussed below:
  - For the QSW-ZVS buck converter, on-off or pulse-width-modulation (PWM) control methods can be used. Considering the lack of commercial controllers for high switching frequency operation, the implemented chip shown in figure 7.5 incorporates a high frequency pulse-width-modulator, which is the vital sub-circuit in the control loop. The chip is also designed to be driven by an on-off (hysteretic) controller.

- For resonant converters, a discrete design of the on-off controller is implemented for a class-DE DC-DC converter switching at 7 MHz. The converter is incorporated in one of the product demonstration boards of Niko Servodan, a TinyPower Project industrial partner, see figure 7.6. It is worth mentioning that an alternative design of the control circuit can be implemented using a frequency-controller.

- Finally, a high-frequency adaptive-deadtime control technique is investigated and implemented in the integrated circuit shown in figure 7.1. A test board is designed and assembled. The test circuit is a Class-DE series-resonant converter. A photograph of the test board is presented in figure 7.5.

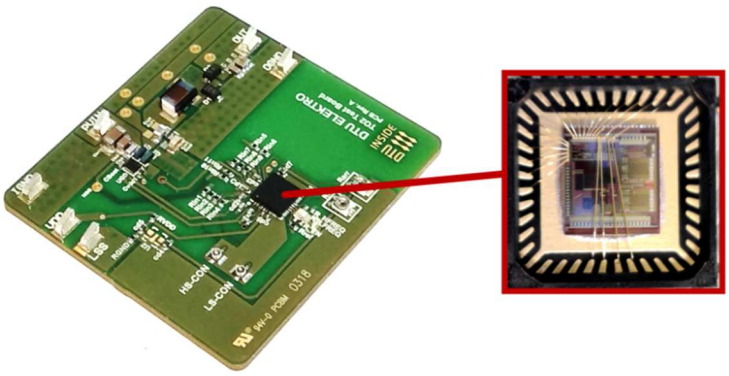


Figure 7.5: An 80 V class-DE resonant converter with a custom designed IC for dead-time control.

Figure 7.6: Niko Servodan's product incorporating the on-off controlled 7 MHz class-DE DC-DC converter (the red box outlines the inverter section of the power stage) [106].

Appendices

List of publications

Patent Applications

A-P1 Yasser Nour and Hoà le Thanh, "A semiconductor substrate member", Feb. 2018.

Journal papers

A-J1 Hoà Thanh Le, Yasser Nour, Zoran Pavlovic, Cian O Mathuna, Flemming Jensen, Anpan Han, Santosh Kulkarni, Ziwei Ouyang, "High-Q 3D Microfabricated Magnetic-core Toroidal Inductors for Power Supplies in Package", submitted to IEEE Transactions on Power Electronics.

A-J2 Jens Christian Hertel, Yasser Nour and Arnold Knott, "Integrated Very High Frequency Switch Mode Power Supplies: Design Considerations," in IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE), 2017.

A-J3 Yasser Nour, Hoa Thanh Le, Anpan Han, Flemming Jensen, Ziwei Ouyang, and Arnold Knott, "Microfabricated Air-core Toroidal Inductor in Very High Frequency Power Converters", IEEE Journal of Emerging and Selected Topics in Power Electronics, 2018.

A-J4 Hoa Thanh Le, Io Mizushima, Yasser Nour, Peter Torben Tang, Arnold Knott, Ziwei Ouyang, Flemming Jensen, and Anpan Han, "Fabrication of 3D Air-core MEMS Inductors for Very-High-Frequency Power Conversion", Journal of Microsystems & Nanoengineering, 2018.

Conference papers

A-C1 Yasser Nour, Arnold Knott, Ivan H. H. Jørgensen, "Investigating Enhancement Mode Gallium Nitride Power FETs in High Voltage, High Frequency Soft Switching Converters," in IEEE International Conference on Power electronics, machines and drives (PEMD), Glasgow, Scotland, 2016.

A-C2 Jens Christian Hertel, Yasser Nour and Arnold Knott, "Very High Frequency Two-Port Characterization of Transistors" e-poster in International Workshop on Power Supply on Chip (PwrSoC), Madrid, Spain, 2016.

A-C3 Yasser Nour, Arnold Knott, and Ivan H. H. Jørgensen, " Implementation of a Dual on Die 140 V Super-Junction Power Transistors" e-poster in International Workshop on Power Supply on Chip (PwrSoC), Madrid, Spain, 2016.

A-C4 Yasser Nour, Ziwei Ouyang, Arnold Knott, Ivan H. H. Jørgensen, "Design and Implementation of High Frequency Buck Converter Using Multi-Layer PCB Inductor", The 42nd Annual Conference of the IEEE Industrial Electronics Society (IECON), Florence, Italy, 2016.

A-C5 Yasser Nour, Arnold Knott, Lars Press Petersen, “High frequency Soft Switching Half Bridge Series-Resonant DC-DC Converter Utilizing Gallium Nitride FETs”, in the 19th European Conference on Power Electronics and Applications, (EPE), Warsaw, Poland, 2017.

A-C6 Hoà Thanh Le, Yasser Nour, Ziwei Ouyang, Arnold Knott, Flemming Jensen, Anpan Han, “3D MEMS Air-core Inductor in a Very High Frequency Switched-Mode Power Converter”, in the 43rd International Conference on Micro and Nano Engineering (MNE), Portugal, 2017.

A-C7 Yasser Nour and Arnold Knott, “Module Integrated GaN Power Stage for High Switching Frequency Operation”, in the 12th IEEE International Conference on Power Electronics and Drive Systems (PEDS), Hawaii, USA, 2017.

A-C8 Christopher Have Kiaerskou Jensen, Frederik Monrad Spliid, Jens Christian Hertel, Yasser Nour, Tiberiu-Gabriel Zsurzsan, and Arnold Knott, “Resonant Full-Bridge Synchronous Rectifier Utilizing 15V GaN Transistors for Wireless Power Transfer Applications Following AirFuel Standard Operating at 6.78MHz”, in the Applied Power Electronics Conference and Exposition (APEC), TX, USA, 2018

A-C9 Sinan Okumus, Lin Fan, Yasser Nour, and Arnold Knott, “Evaluation of custom-designed lateral power transistors in a silicon-on-insulator process in a synchronous buck converter”, International Conference on Renewable Energies and Power Quality (ICREPQ’18) - Salamanca, Spain, 2018.

Appendix A-P1

Yasser Nour and Hoà le Thanh, "A semiconductor substrate member", Feb. 2018.

A semiconductor substrate member

Semiconductor substrate components are widely used to closely integrate a few to millions of semiconductor components such as transistors, diodes, resistors, capacitors or even inductors to form much more complex circuits like central processing units, CPUs, microcontrollers and a wide range of other devices like modems for wired or wireless communication.

However, oftentimes it is necessary to electrically connect external passive components such as inductors and capacitors to the semiconductor components. In connection therewith, it is observed that there is an unmet demand for further closely integrating electrical circuits.

A special technical field, where there is such an unmet demand for closely integrating electrical circuits, is the field of power supply units, such as DC-to-DC converter units, which are typically based on switched-mode power conversion.

Typical requirements for a power supply unit, in general, are: low cost, light weight, high degree of reliability, efficient power conversation, and small size. Further typical requirements are modularity and being "easy to use".

With the earliest switched-mode power converters, it became clear that higher switching frequencies allow smaller inductors and capacitors. This in turn should lead to smaller, lighter, and less costly systems. Smaller inductors and capacitors generally contribute to higher power densities. Power density may be defined as electrical power per volume unit, such as [W/mm^3], which represents rated electrical power input to or output from a power converter divided by the cubic space of the power converter.

However, using a high switching frequency is not enough to achieve higher power densities. Also, a high switching frequency may come at the cost of decreased efficiency of the switched-mode power converter since parasitic components play an increasing role with increasing switching frequency.

New devices need to be developed to achieve a goal such as higher power density.

In general, it should be appreciated that a semiconductor substrate member is a piece of substrate which may have embedded therein, by a semiconductor manufacturing process, one or more semiconductor components.

In contrast thereto, semiconductor substrate member may carry one or more components attached to the semiconductor substrate member e.g. by soldering or wire-bonding or another bonding technique. This is typically performed by (during) montage or mounting, such as surface mounting.

Also, it should be appreciated that a semiconductor substrate member may be attached to one or more other semiconductor substrate members e.g. in a stack. Further, a semiconductor substrate member may be attached to a printed circuit board, PCB; which may have one or more metal layers supported by layers of e.g. a glass-fibre reinforced epoxy material.

Generally, it is known that wire-bonding connections introduces parasitic inductances and resistances and behaves as antennas transmitting electromagnetic radiation which easily causes problems related to electromagnetic interference, EMI, especially at (high) switching frequencies.

Generally, stray electromagnetic fields are known to cause problematic Electromagnetic Interference, EMI. Especially, switched circuits, such as switched power supplies like DC-to-DC converters and switched power amplifiers like class-D power amplifiers, are prone to cause EMI problems.

Generally, it is known that so-called flip-chipping, which is a technique used for surface mounting semiconductor substrate members to e.g. printed circuit boards, has its limitations in terms of stacking components since a semiconductor substrate member for flip-chipping has only one side available for mounting.

Generally, in the field of power converters circuit architectures fully or partially implemented in a silicon substrate as a small-sized module, it is known that the term PSiP designates “Power Supply in a Package” and the term PwrSoC designates “Power Supply on a Chip”.

RELATED PRIOR ART

US 8,907,447 discloses an inductor integrated in a semiconductor substrate for use in a DC-DC converter. Such an inductor is sometimes referred to as a power inductor in silicon. In an embodiment, the inductor has a magnetic core of magnetic material embedded in a silicon substrate and a conductive winding. The inductor is a spiral inductor, or a toroidal inductor integrated in the substrate. A cap layer of magnetic material is disposed on at least one side of the silicon substrate to increase the inductance of the inductor. It is also described that the DC-DC converter includes an integrated circuit mounted on top of the cap layer of the power inductor in silicon. However, despite of having a small size, there is still a need for more integration and improved efficiency of such DC-DC converters. Also, The process used for manufacturing the inductors is not compatible with semiconductor processes which makes it harder to integrate active devices and other passive devices in the same substrate for tighter integration.

KR 10-0438892 discloses a one-chip module package by forming an integrated circuit and a thin film inductor in the same semiconductor substrate. A first and a second well region are formed in a semiconductor substrate. A first and a second MOS (Metal Oxide Semiconductor) transistor are formed on the first and second well region, respectively. A plurality of metal layer patterns are electrically connected between the first and second MOS transistor and impurity regions. A protecting isolation layer is located on the resultant structure for separating the metal layer patterns. A lower core layer pattern is formed on the predetermined portion of the protecting isolation layer. The first polyimide layer, a metal coil layer, the second

polyimide layer, an upper core layer pattern, and the third polyimide layer are sequentially formed on the resultant structure.

Most of the prior art on integrated power supplies use either on-silicon inductors or in-silicon inductors fabricated by 2D semiconductor fabrication technologies. 2D semiconductor fabrication technologies are limited to planar inductor geometries, such as circular spirals, rectangular spirals, and elongated spirals (so-called racetrack inductors) – all of which induces strong stray electromagnetic fields perpendicular to the inductor plane. This is a problem towards closer integration of components since the stray electromagnetic fields, perpendicular to the inductor plane, interferes with other components, such as active semiconductor devices, integrated in proximity of the inductor, whereby electromagnetic interference (EMI) is likely to become an issue.

Thus, there is still a need for a small-size one-chip module package which enables tight integration and reduced stray electromagnetic fields.

SUMMARY

It is realized that a fully functional power converter, such as a DC-to-DC converter can be embodied on a single semiconductor substrate member with a thickness of less than a millimetre including all active and passive components needed. There is provided:

A semiconductor substrate member, comprising:

- a first region with a passive electrical component with a first electrically conductive layer pattern of an electrically conductive material and a second electrically conductive layer pattern of an electrically conductive material deposited on respective sides of the semiconductor substrate member; wherein a trench or a through-hole is formed in the substrate within the first region, and wherein the electrically conductive material is deposited at least on a bottom portion of the trench or on a sidewall of the through-hole and

electrically connected to one or both of the first conductive layer pattern and the second conductive layer pattern; and

- a second region with an active semiconductor component embedded in the semiconductor substrate member by a semiconductor fabrication process.

Such a semiconductor substrate member enables the manufacture of thin power supplies which are suitable for products which require very tight integration of its components, such as in mobile devices e.g. smart-phones, smart-watches etc. Oftentimes, such products require a certain degree of Electromagnetic Compatibility, EMC, to ensure proper functioning of advanced circuitry inside the product.

Such a semiconductor substrate member enables better inductor topologies such toroidal inductors and solenoid inductors, compared to spiral inductors. This may be attributed to the geometry enabling an improved quality factor (related to storing of energy to losses ratio) of the inductor.

Such a semiconductor substrate member can be made much smaller that corresponding components on a Printed Circuit Board and with much smaller tolerances, which in turn reduces parasitic elements and hence enables use of higher switching frequencies e.g. in a power supply module such as DC-DC converter.

Especially, it is possible to reduce electromagnetic field radiation from the semiconductor substrate member. The passive components have a 3D, three-dimensional, configuration extending not only as electrical paths at the surface of the semiconductor substrate member in one or both of a horizontal top and bottom plane, but also with electrical paths through the semiconductor substrate member in a vertical direction. Thus, forming a 3D, three-dimensional, configuration. This enables to a higher degree, than for planar passive components, to keep electromagnetic fields, at least where they are strongest, inside the volume of the semiconductor substrate member.

The active semiconductor component embedded in the semiconductor substrate member may be fabricated e.g. by a Silicon, Gallium-nitride, or Gallium-arsenide semiconductor fabrication process. The semiconductor fabrication process may be a conventional semiconductor manufacturing process where a semiconductor wafer is used as a starting material for the manufacturing process. The process may involve etching, deposition of implants such as a so-called dopant like Boron and Phosphorus to form active devices like transistors and diodes, and deposition of metal one or more layers to form interconnects among the active components. The result of the process is a processed wafer with active components.

The processed wafer with active components is passivated by one or more protective layers to protect the active components from post processing steps.

Post processing steps are applied to form the passive components. Post processing steps may include etching to form trenches and through-holes and deposition to apply one or more metal layers to form the passive components. The one or more metal layers are formed e.g. at the through-holes to form through-substrate vias (TSVs) and/or at the one or more trenches and/or between the passive component and the one or more active components to form the electrically conductive layer pattern and/or at pads for soldering or wire-bonding to attach additional component members. One or more steps of post processing is to establish electrical connection between the passive components and the active components by deposition of a metal layer; this may include removing the protective layer fully or partially to enable electrical connection with the active components. The result of post processing is the semiconductor substrate member. The semiconductor substrate member may implement a power supply, a power amplifier or another integrated circuit comprising active and passive components.

Following post-processing, the semiconductor substrate member is manufactured and may be subject to assembly steps e.g. for being attached to a so-called lead-frame and/or a PCB and/or for having component members, such as SMD components attached to it by soldering. Also, component members may be attached by wire-bonding.

Manufacturing of a semiconductor substrate member with a structure as set out in the claims and generally described herein can be performed with a conventional semiconductor manufacturing process method and a method for manufacturing a hollow MEMS structure e.g. as described in WO 2017/108218-A1 assigned on its face to Danmarks Tekniske Universitet.

The thickness of the semiconductor substrate member may be e.g. about 280 um, 350 um, 500, 1100 um. The member may have a rectangular shape and be e.g. 6 by 9 mm or larger or smaller. The member may also have another shape e.g. circular or oval.

The first region and the second region may abut one another e.g. at a transverse or longitudinal border across the semiconductor substrate member. The first region and the second region may be spatially non-overlapping. The first region and the second region may have any shape and may have a mutually spatially complementary shape.

Depositing comprises one or more of electro-deposition, sputtering, evaporation, atomic layer deposition.

The semiconductor components may be in accordance with complementary metal-oxide-semiconductor (CMOS) technology. The power supply may be implemented as a so-called interposer, which may be arranged between an application printed circuit board (PCB) and an integrated circuit (IC). The interposer may establish conductive vias or paths between the PCB and the IC.

Further embodiments are described in the detailed description.

There is also provided a stack of components comprising one or more semiconductor substrate members as set out herein, wherein at least one semiconductor substrate member comprises pad portions on a top side and pad portions on a bottom side.

A stack of components may comprise: a first semiconductor substrate member and a second semiconductor substrate member. A stack of components may additionally comprise one or more of: a PCB, one or more further semiconductor substrate members, and more or more discrete components such as passive components and/or active components. The components may be surface-mount components. The components in the stack may be attached to each other at the pad portions by soldering or gluing.

There is also provided a DC-DC converter comprising a semiconductor substrate as described herein.

The DC-DC converter may have a configuration selected from the group of: Buck-converters, boost converters, and fly-back converters. The converters may be step-up or step-down converters. The converter may be a resonant converter. The DC-DC converter may be configured for voltages up to 10 volts or higher, e.g. 48 volts. The DC-DC converter may be configured to power levels of up to 20-30 Watts or higher.

BRIEF DESCRIPTION OF THE FIGURES

A more detailed description follows below with reference to the drawing, in which:

fig. 1 shows a perspective view of a semiconductor substrate member with a first region with a passive electrical component and a second region with an active semiconductor component integrated with the semiconductor substrate member;

fig. 2 shows a perspective view of the semiconductor substrate member of fig. 1 with additional component members mounted on one side of the semiconductor substrate member;

fig. 3 shows a perspective view of a solenoid inductor embedded in the semiconductor substrate member;

fig. 4 shows a perspective view of a winding of an inductor embedded in the semiconductor substrate member;

fig. 5 shows a perspective view of a first coil and a second coil of an inductive transformer or a coupled inductor with coupled coils which can be embedded in the semiconductor substrate member;

fig. 6 shows a perspective view of the toroidal inductor embedded in the semiconductor substrate member and having a inductor core which has an array of deep trenches.

fig. 7 shows a cross-sectional view of the inductor core which has an array of deep trenches;

fig. 8 shows a cross-sectional view of a trench, of an inductor core, filled with a magnetic material;

fig. 9 shows a cross-sectional view of a trench, in an inductor core, filled with a magnetic material or magnetic particles suspended in epoxy;

fig. 10 shows a cross-sectional view of a trench, in an inductor core, laminated with a first layer of a magnetic material and a second layer of a non-magnetic material;

fig. 11 shows a perspective view of the capacitor embedded in the semiconductor substrate member and cross-sectional views, A-A and B-B thereof;

fig. 12 shows a cross-sectional view of another capacitor, which can be embedded in the semiconductor substrate member; and

fig. 13 shows cross-sectional view of yet another capacitor, which can be embedded in the semiconductor substrate member.

DETAILED DESCRIPTION

In some embodiments, the semiconductor substrate member is embodied as power supply in a package, PSiP, embodied as a micro-fabricated 3D passive interposer. The micro-fabricated 3D passive interposer may have a size less than about 40 by 40 by 1 mm, e.g. about 4 by 8 by 0.3 mm, and comprise 3D toroidal inductor with through-substrate vias, TSVs, and through-substrate vias establishing interconnects from one side of the micro-fabricated 3D passive interposer to the other. The power supply in a package may comprise a Buck converter or a Class DE resonant converter. The power supply in a package may comprise active components, such as one or more Field Effect Transistors, FETs, one or more gate drivers, and capacitors. The power supply in a package may operate in accordance with zero-voltage switching (ZVS), e.g. in accordance quasi-square wave (QSW) mode, to convert a first DC voltage, e.g. about 5 VD, to a second DC voltage e.g. about 3.3 VDC. The power supply in a package may operate at a switching frequency above 5 MHz e.g. at about 22 MHz. The power supply in a package may comprise a 3D air-core toroidal inductor e.g. of about 50-nH. However, the claims are not limited thereto. A Buck-type converter, power supply in a package, was successfully tested with an output current from 0 to 300 mA and an input voltage from 3.5 to 8.5 V. A peak efficiency of 83.0 % at 300 mA output current was measured and a 1.15 Watts was delivered to a load.

In some embodiments one or both of the first electrically conductive layer pattern and the second electrically conductive layer pattern extends across at

least some of second region to electrically connect the active semiconductor component with the passive electrical component.

In this way the path of the electrical connection between the active component and the passive component can be made shorter and less prone to generating electromagnetic interference, EMI. Also parasitic elements can be reduced.

Then interconnection between the active component and the passive component doesn't have to go via the PCB. This in turn reduces electromagnetic field radiation. Also, costs related to assembling may be reduced.

It should be noted that the one or both of the first electrically conductive layer pattern and the second electrically conductive layer pattern extends in parallel horizontal planes e.g. at opposite (top and bottom) sides of the semiconductor substrate member. However, one or both of the first electrically conductive layer pattern and the second electrically conductive layer pattern may follow topography, such as a submicron-topography of the semiconductor substrate member.

In some embodiments the one or both of the first electrically conductive layer pattern and the second electrically conductive layer pattern comprises a pad portion which is exposed for electrical connection by soldering, wire bonding or flip-chip bonding.

Thereby, the semiconductor substrate member is configured for use as an combined active-passive interposer. The pad portion enables interconnection with other components and/or a PCB by soldering or wire-bonding. In some embodiments the semiconductor substrate member comprises pad portions on both a top side and a bottom side which enables stacking of multiple semiconductor substrate members.

Soldering may comprise using a solder paste or solder ball to electrically connect by heating to melt the solder.

Wire-bonding may comprise attaching a wire to the pad portion by applying sufficient pressure and/or heat e.g. by ultrasound. The wire for wire-bonding may comprise a metal such as gold, aluminium, or copper as it is known in the art.

Flip-chip bonding may comprise attaching a substrate to a PCB or another substrate by forming a ball or pillar of metal and gluing with an electrically conductive glue the ball or pillar to the substrate and the PCB or the other substrate.

In some embodiments one or both of the first electrically conductive layer pattern and the second electrically conductive layer pattern comprises a portion, extending from or to the pad portion, which is covered by an isolation layer. The isolation layer may be e.g. silicon oxide (SiO_2), aluminium oxide (Al_2O_3), or silicon nitride (Si_3N_4). The isolation layer may be applied using methods known in the art.

In some embodiments the semiconductor substrate member comprises an inductor formed in the first region with an inductor winding of the inductor comprising:

- a first winding portion formed in the first electrically conductive layer pattern,

- a second winding portion formed by a first through-substrate-via,

- a third winding portion formed in the second electrically conductive layer pattern, and

- a fourth winding portion formed by a second through-substrate-via;

wherein the first, second, third and fourth portions are electrically connected by the deposited electrically conductive material.

Thereby a 3D inductor is formed. Such a 3D inductor may emit a significantly reduced electromagnetic field in a direction normal to the top and bottom surface of the semiconductor substrate member compared to a planar, e.g. spiral-shaped, inductor. Instead, the claimed inductor may have an electromagnetic field which is concentrated inside the volume of the semiconductor substrate member.

In some embodiments the inductor is a solenoid inductor or a toroidal inductor.

In some embodiments an inductor winding circumscribes an inductor core, comprising a material selected from the group of: air, silicon, magnetic materials, epoxy or a combination thereof.

In some embodiments an inductor winding circumscribes an inductor core, comprising magnetic particles suspended in epoxy. The epoxy material establishes spacing between the magnetic particles, thereby reducing eddy current loss. Thereby it is possible to strike a trade-off between an inductor with an air core known to have low loss, low inductance and a magnetic core known to have high loss, high inductance.

In some embodiments an inductor winding circumscribes an inductor core which has an array of deep trenches filled with or laminated with a magnetic material or magnetic particles suspended in epoxy. The array may comprise one or more rows of deep trenches. A core may comprise an array with e.g. 10 to 500 deep trenches.

In some embodiments an inductor winding circumscribes an inductor core which has an array of deep trenches laminated with a first layer of a magnetic material and a second layer of a non-magnetic material. Thereby, the non-magnetic layer reduces eddy current loss since magnetic layers are separated by the non-magnetic layer. Thereby it is possible to strike a trade-off between an inductor with an air core known to have low loss, low

inductance and a magnetic core known to have high loss, high inductance. Thereby vertical laminar layers are established.

In some aspects, the semiconductor substrate member comprises a layer or patch of an electrically non-conductive material (dielectric) at least covering some openings of the deep trenches when the trenches are laminated. In some aspects the layers are deposited by electro-deposition or atomic layer deposition.

In some embodiments the inductor comprises a first coil and a second coil circumscribing a common inductor core, wherein windings of the first coil and windings of the second coil are formed by the first electrically conductive layer pattern and the second electrically conductive layer pattern and through-substrate vias. It should be noted that “windings” are windings of an inductor formed by depositing an electrically conductive material, rather than by winding a thread about the core.

A "through-substrate via" is a via formed by firstly etching a hole through the semiconductor substrate member and then depositing an electrically conductive material to establish electrical connection from one side of the semiconductor substrate member to the opposite side e.g. extending between pads at the opposite sides. The electrically conductive material should be electrically isolated from the substrate material.

In some embodiments the semiconductor substrate member comprises a capacitor formed by:

- a first capacitor member which comprises a conductive material deposited in first deep trenches extending from a first side of the semiconductor substrate; and

- a second capacitor member which comprises a conductive material deposited in second deep trenches extending from a second side of the semiconductor substrate.

The conductive material deposited in the deep trenches extending from the first side of the semiconductor substrate is electrically connected to the first electrically conductive layer pattern, and the conductive material deposited in the deep trenches extending from the second side of the semiconductor substrate is electrically connected to the second electrically conductive layer pattern.

Reverting to the detailed description:

Fig. 1 shows a perspective view of a semiconductor substrate member with a first region with a passive electrical component and a second region with an active semiconductor component integrated with the semiconductor substrate member. The semiconductor substrate member 101 has a substantially plate-shaped form. For convenience the size of the semiconductor substrate member 101 may be designated by a length along an x-axis, a width along a y-axis, and a height along a z-axis, as shown. Also, for convenience, the length and width are defined in a horizontal plane and the height in a vertical direction. Further, for convenience, a top side refers to one side 107 of the semiconductor substrate member (e.g. the one facing upwards in the figure) and a bottom side refers to the opposite side 108 of the semiconductor substrate member (e.g. the one facing downwards in the figure).

The semiconductor substrate member 101 has a first region 102 and a second region 103 which may be both defined in the horizontal plane. The regions may be associated with respective end-portions of the semiconductor substrate member or with another geometrical definition. The semiconductor substrate member may have a rectangular shape, a polygonal shape, a circular or oval shape or a combination thereof. Also, the first region 102 and the second region 103 may have a rectangular shape, a polygonal shape, a circular or oval shape or a combination thereof.

One or more passive electrical components 104, e.g. selected from the group of inductors, capacitors and resistors, may be accommodated within the first region 102.

One or more active semiconductor components 111 may be integrated within a second region 103 of the semiconductor substrate member 101 by being fabricated by a semiconductor fabrication process. The active semiconductor components may be selected from the group of transistors, diodes or any devices fabricated by a conventional semiconductor fabrication process. As it is known in the art, the semiconductor fabrication process may restrict transistors and diodes within the certain types e.g. CMOS types or bipolar types. It should be noted that the one or more active semiconductor components 111 are depicted as a rectangular 3D space, however, as it is known within the field of semiconductors, multiple semiconductor components – such as arrays of semiconductor components may be arranged and electrically interconnected in such a 3D space, irrespective of its shape.

One or more first electrically conductive layer patterns 105 of an electrically conductive material and one or more second electrically conductive layer patterns 106 of an electrically conductive material may be deposited on respective sides 107, 108 of the semiconductor substrate member 101. The one or more first electrically conductive layer patterns 105 and the one or more second electrically conductive layer patterns 106 serves to electrically connect one or more passive components within the first region with one or more active components within the second region. Additionally, or alternatively, the electrically conductive layer patterns 106, 107 form at least portions of the one or more passive components. The portions of the one or more passive components may be one or more of e.g. portions of inductor windings and portions of capacitor plates. In this respect the term 'windings' should be construed as being a winding of an inductor which is not "winded" as a thread, but rather a structure of an inductor. Further, the term 'capacitor

plates' or simply 'plates' should be construed as serving the function of a capacitor plate, rather than necessarily having a plate-shape.

The semiconductor substrate member 101 has one or more, such as multiple, trenches 109 or through-holes 110 etched into, such as through, the semiconductor substrate member 101. The trenches 109 or through-holes 110 are formed by an etching process, removing semiconductor material from the semiconductor substrate member within the first region. Subsequently, electrically conductive material is deposited at least on a bottom portion of a trench or on a sidewall of the through-hole to electrically connect to one or both of the first conductive layer pattern 105 and the second conductive layer pattern 106.

In this way, one or more passive components can be formed and electrically connected to the one or more active components.

It should be known that one or more pad portions 112 may be arranged on a bottom side and/or on a top side of the semiconductor substrate member to connect to the first electrically conductive layer pattern and/or second electrically conductive layer pattern and/or to provide for mechanical support e.g. by soldering to another member such as a PCB.

An isolation layer 113 is deposited to electrically isolate the one or more conductive layers from the semiconductor material.

In some embodiments the semiconductor substrate member 101 has a size of approximately 4-by-8 mm and thickness of about 280 µm. However, the semiconductor substrate member 101 may be larger or smaller than that e.g. up to 40-by40 mm and with thickness of about 200 µm to1100 µm.

Fig. 2 shows a perspective view of the semiconductor substrate member of fig. 1 with additional component members mounted on one side of the semiconductor substrate member. Here, it is shown that the semiconductor substrate member 101 accommodates stacked, passive electrical

components 133. The stacked, passive electrical components 133 may be attached to the semiconductor substrate member by surface-mount soldering. It should be noted however, that the semiconductor substrate member 101 may accommodate stacked, active electrical components.

It should be noted that the stacked, passive electrical components 133 or the stacked, active electrical components may be denoted discrete components in the sense that they are not integrated in the semiconductor substrate member.

It should be noted that the discrete components can be arranged anywhere on the semiconductor substrate member when attached at pad portions to connect to circuitry integrated with the semiconductor substrate member.

Fig. 3 shows a perspective view of a solenoid inductor embedded in the semiconductor substrate member. The solenoid inductor 124 may be used as an alternative or in addition to the toroidal inductor. It should be noted that the semiconductor substrate member is shown only partially, not including the first region 102 which accommodates the one or more active semiconductor components.

The solenoid inductor 124 is electrically connected with one or both first electrically conductive layer pattern 105 and the second electrically conductive layer pattern 106 (not shown here). Thereby a 3D solenoid inductor is provided in the semiconductor substrate member 101.

Fig. 4 shows a perspective view of a winding of an inductor embedded in the semiconductor substrate member. The winding 144 may be a winding of a solenoid inductor or a toroidal inductor. Multiple windings 144 are arranged next to each other and are electrically connected to form an inductor as it is known in the art.

The winding 144 comprises a first winding portion 114 formed in the first electrically conductive layer pattern, a second winding portion 115 formed by

a first through-substrate-via, a third winding portion 116 formed in the second electrically conductive layer pattern, and a fourth winding portion 117 formed by a second through-substrate-via. The first, second, third and fourth portions are electrically connected by the deposited electrically conductive material.

In particular, it should be noted that one or both of the second winding portion 115 and the fourth winding portion 117 may comprise one or more first through substrate vias, TSVs. The through substrate vias may have e.g. a substantially circular cross-section or have a substantially rectangular cross-section. The latter example can be described as a "vertical wall" rather than cylinders as shown.

Fig. 5 shows a perspective view of a first coil and a second coil of an inductive transformer with coupled coils which can be embedded in the semiconductor substrate member. The inductive transformer is configured as a toroidal inductive transformer and comprises a first coil 126 and a second coil 127 circumscribing a common inductor core. The first coil 126 is shown with relatively "wider" windings than the second coil 127, which has relatively "narrower" windings than the first coil 126. The first coil 126 and the second coil 127 are electrically isolated from each other. The windings "cross" each other at respective sides of the semiconductor substrate member, but not at the same side. Thus, with reference to the winding 144, for the first coil 126, a first winding portion 114 formed in the first electrically conductive layer pattern, "crosses" a respective third winding portion 116 of the second coil 127. One or both of the width and thickness of a winding of a respective coil, may be configured to carry a respective desired amount of electrical current.

Fig. 6 shows a perspective view of the toroidal inductor embedded in the semiconductor substrate member and having an inductor core which has an array of deep trenches. For illustration purposes the semiconductor substrate member is partially cut away to better show the inductor core, which has an array of deep trenches 119.

As shown the deep trenches 119 are arranged as concentric, curved "vertical walls" to collectively substantially fit the space available within the core of the toroidal inductor or transformer as the case may be. The curved "vertical walls" are spaced apart in a direction normal to the wall. The walls may be divided into angular sections.

Fig. 7 shows a cross-sectional view of the inductor core which has an array of deep trenches. The cross-sectional view is also a cross-section of a portion of the semiconductor substrate member 101. The uppermost portion shown is an isolation layer 113, which isolates an electrically conductive material deposited in the deep trenches 119 in the inductor core from one or more first electrically conductive layer patterns (not shown here) and from the semiconductor substrate 101.

Fig. 8 shows a cross-sectional view of a trench, of an inductor core, filled with a magnetic material. The magnetic material is deposited in a deep trench laminated with an isolation layer 113 which isolates an electrically conductive material deposited in the deep trenches 119 in the inductor core from one or more first electrically conductive layer patterns (not shown here) and from the semiconductor substrate 101.

Fig. 9 shows a cross-sectional view of a trench, in an inductor core, filled with a magnetic material or magnetic particles suspended in an epoxy material. The magnetic material or magnetic particles suspended in an epoxy material is designated by reference numeral 120.

Fig. 10 shows a cross-sectional view of a trench, in an inductor core, laminated with a first layer of a magnetic material and a second layer of a non-magnetic material. The first layer 122 of a magnetic material is arranged alternately with a second layer 123 of a non-magnetic material. The layers may continue substantially horizontally at the bottom of the trench to connect vertical layers at the side or sides of the trench – alternatively, the vertical

layers may terminate at the bottom of the trench with end portions of the vertical layers abutting a bottom portion of the trench.

Fig. 11 shows a perspective view of the capacitor embedded in the semiconductor substrate member and cross-sectional views, A-A and B-B thereof. The capacitor has a first terminal 136 and a second terminal 137. The first terminal 136 and the second terminal 137 faces the same side of the semiconductor substrate member 101, but could also face opposing sides.

The "capacitor plates" are implemented as deep trenches wherein an electrical conductive material is deposited to form an array of parallel "vertical walls" or "lamella" alternately electrically connected to the first terminal 136 and the second terminal 137 and alternately electrically isolated from the first terminal 136 and the second terminal 137. Otherwise, the parallel "vertical walls" are electrically isolated from each other.

Cross-sectional view, A-A, shows that the first electrically conductive layer pattern 105, of which a portion may form a portion of the first capacitor member 129, is arranged between isolation layers 113. One or more of the isolation layers may extend along sides and bottom of the deep trenches and across the semiconductor substrate member between the deep trenches e.g. to form a substantially coherent layer. The first electrically conductive layer pattern 105, of which a portion may form a portion of the first capacitor member 129, may be deposited to form capacitor plates and to mutually connect the capacitor plates. Atop the first electrically conductive layer pattern 105, another one or more of the isolation layers may be deposited. One or more portions of the isolation layers may be removed e.g. by etching to expose electrical connection to the first electrically conductive layer pattern 105 e.g. as shown at pad portion 112 at the top-side.

Correspondingly, at the bottom side, the second electrically conductive layer pattern 106, one or more portions of the isolation layers may be removed e.g. by

etching to expose electrical connection to the second electrically conductive layer pattern 106 e.g. as shown at pad portion 112 at the bottom side.

Cross-sectional view, B-B, shows essentially the same structure as shown in cross-sectional view, A-A. It can be inferred that the capacitor plates connected to respective capacitor terminals do not fully overlap, but rather are displaced relative to each other longitudinally. However, various configurations of the capacitor plates are foreseeable, e.g. comprising that the capacitor plates fully overlap in a longitudinal direction.

The isolation layers 113 also provides electrical isolation between the capacitor plates and the semiconductor substrate.

Fig. 12 shows a cross-sectional view of another capacitor, which can be embedded in the semiconductor substrate member. This configuration of a capacitor is suitable for implementing capacitors with relatively narrow trenches, which may be difficult to reliably made deep in the sense that they extend through the full depth (thickness) of the semiconductor substrate. An unfilled trench 139 may reduce the thickness of the substrate at the area where the capacitor is embedded.

As shown, the wide and unfilled trench 139 is formed in the substrate from the top-side of the semiconductor substrate member. Inside the trench is deposited a portion of the first capacitor member 129 as a layer of conductive material, which electrically is connected to the first electrically conductive layer pattern 105.

The capacitor is formed by realizing non-overlapping deep trenches from both top and bottom side of the substrate. Isolating layer 113 is applied on the top side bottom side and inside the trenches. Conductive layer from top 105 is deposited to for the first plate of the capacitor 131. The second plate of the capacitor 132 is realized by depositing a conductive layer 106 on the back side of the substrate. Another Isolation layer 113 may be deposited on

top and bottom of the substrate. Pads or pad openings 112 may be realized by etching the isolation layer for external connections.

The deep trenches are laminated with an isolation layer 138 to isolate capacitor plates of different polarity from each other and serves as the dielectric material of the capacitor. The isolation layer 138 may be made from a material that has a different dielectric constant than the material of the isolation layer 113. The material of the isolation layer 138 may have a dielectric constant larger than e.g. 12 and to about 150 or up to about 200 or higher. The material of the isolation layer 138 may be a ceramic e.g. titanium-oxide, which has may have a dielectric constant in the range of 86 to 173. The material of the isolation layer 113 may be for example silicon-oxide or Aluminium-oxide.

Fig. 13 shows cross-sectional view of yet another capacitor, which can be embedded in the semiconductor substrate member. The capacitor is formed by realizing non-overlapping deep trenches from both top and bottom side of the substrate. Isolating layer 113 is applied on the top side bottom side and inside the trenches. Conductive layer from top 105 is deposited to for the first plate of the capacitor 131. The second plate of the capacitor 132 is realized by depositing a conductive layer 106 on the back side of the substrate. Another Isolation layer 113 may be deposited on top and bottom of the substrate. Pads or pad openings 112 may be realized by etching the isolation layer for external connections.

A prototype of the device integrates two 40 V gallium-nitride field effect transistors (GaNFETs) driven by a high frequency half bridge gate driver and an in-silicon inductor in addition to input and output capacitors. The in-silicon inductor could be fabricated with a nonmagnetic-core (e.g. air core, non-conducting thermal conducting polymers) or integrated magnetic core (e.g. composite core by screen-printing, electroplated solid/laminated core). All the

mounted components are commercially available. The prototype device is configured as a zero-voltage switching buck converter power stage.

The proposed converter uses a CMOS compatible process to construct 3D passive components without affecting the active part of the silicon die. As an added value, the top side of the silicon die can be used to integrate the components which are not compatible with integrated circuits processing like Gallium nitride FETs, Ceramic capacitors, etc. The mounted components are connected to the silicon devices using through silicon vias (TSVs) and/or conductive layers. The toroidal core can be fabricated with a wide range of core materials: air, silicon, non-conducting thermal polymers, composite core (micro or nanoscale magnetic powders mixed in a non-conducting thermal polymer), micro-fabricated magnetic material (magnetic thin films, lamination thin films, deep-trench magnetic).

The proposed converter allows the lowest profile converters (basically silicon wafer thickness if no stacked components are used). Lower noise converters are possible with technology due to shorter current loops and compact size.

CLAIMS

1. A semiconductor substrate member (101), comprising:

- a first region (102) with a passive electrical component (104) with a first electrically conductive layer pattern (105) of an electrically conductive material and a second electrically conductive layer pattern (106) of an electrically conductive material deposited on respective sides (107, 108) of the semiconductor substrate member; wherein a trench (109) or through-hole (110) is formed in the substrate within the first region, and wherein the electrically conductive material is deposited at least on a bottom portion of the trench or on a sidewall of the through-hole and electrically connected to one or both of the first conductive layer pattern (105) and the second conductive layer pattern (106); and

- a second region (103) with an active semiconductor component (111) embedded in the semiconductor substrate member (101) by a semiconductor fabrication process.

2. A semiconductor substrate member according to claim 1, wherein one or both of the first electrically conductive layer pattern (105) and the second electrically conductive layer pattern (106) extends across at least some of second region (103) to electrically connect the active semiconductor component (111) with the passive electrical component (104).

3. A semiconductor substrate member according to claim 1 or 2, wherein the one or both of the first electrically conductive layer pattern (105) and the second electrically conductive layer pattern (106) comprises a pad portion (112) which is exposed for electrical connection by soldering, wire bonding or flip-chip bonding.

4. A semiconductor substrate member according to any of the preceding claims, wherein one or both of the first electrically conductive layer pattern (105) and the second electrically conductive layer pattern (106) comprises a portion, extending from or to the pad portion (112), which is covered by an isolation layer (113).

5. A semiconductor substrate member according to any of the preceding claims, comprising an inductor (124; 125) formed in the first region with an inductor winding of the inductor comprising:

- a first winding portion (114) formed in the first electrically conductive layer pattern,

- a second winding portion (115) formed by a first through-substrate-via,

- a third winding portion (116) formed in the second electrically conductive layer pattern, and

- a fourth winding portion (117) formed by a second through-substrate-via;

wherein the first, second, third and fourth portions are electrically connected by the deposited electrically conductive material.

6. A semiconductor substrate member according to claim 5, wherein the inductor is a solenoid inductor (124) or a toroidal inductor (125).

7. A semiconductor substrate member according to claim 5 or 6, wherein an inductor winding circumscribes an inductor core (118), comprising a material

selected from the group of: air, silicon, magnetic materials, epoxy or a combination thereof.

8. A semiconductor substrate member according to any of claims 5-7, wherein an inductor winding circumscribes an inductor core (118), comprising magnetic particles suspended in epoxy.

9. A semiconductor substrate member according to any of claims 5-8, wherein an inductor winding circumscribes an inductor core (118) which has an array of deep trenches (119;120;121) filled with or laminated with a magnetic material or magnetic particles suspended in epoxy.

10. A semiconductor substrate member according to any of claims 5-9, wherein an inductor winding circumscribes an inductor core (118) which has an array of deep trenches (121) laminated with a first layer (122) of a magnetic material and a second layer (123) of a non-magnetic material.

11. A semiconductor substrate member according to any of claims 5-10, wherein the inductor comprises a first coil (126) and a second coil (127) circumscribing a common inductor core, wherein windings of the first coil and windings of the second coil are formed by the first electrically conductive layer pattern and the second electrically conductive layer pattern and through-substrate vias.

12. A semiconductor substrate member according to any of the preceding claims, comprising a capacitor (128) formed by:

- a first capacitor member (129) which comprises a conductive material deposited in first deep trenches (131) extending from a first side of the semiconductor substrate; and

- a second capacitor member (130) which comprises a conductive material deposited in second deep trenches (132) extending from a second side of the semiconductor substrate.

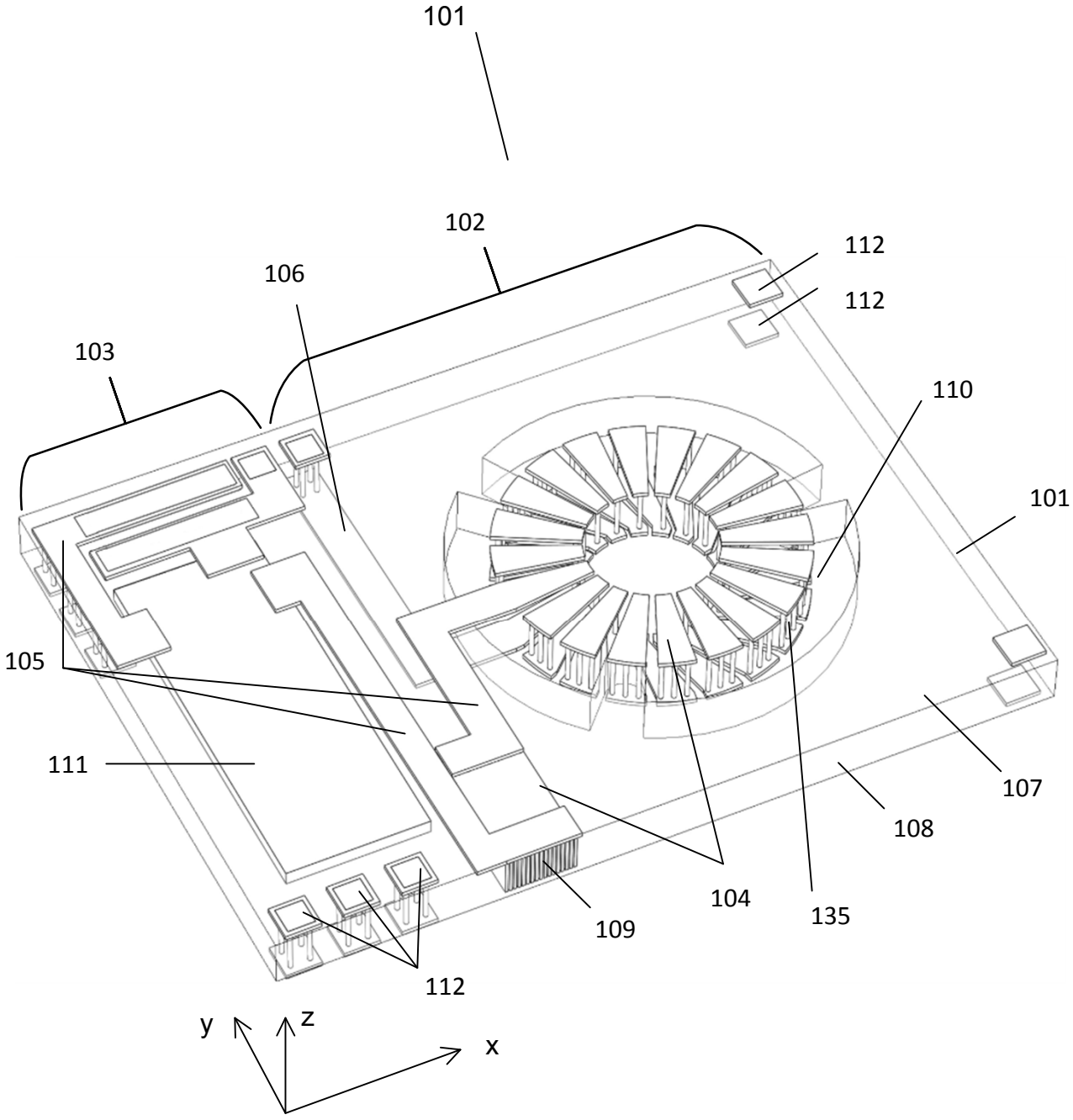
13. A stack of components comprising one or more semiconductor substrate members according to any of the preceding claims, wherein at least one semiconductor substrate member comprises pad portions (112) on a top side and pad portions (112) on a bottom side.

14. A DC-DC converter comprising a semiconductor substrate according to any of claims 1-13.

ABSTRACT

A semiconductor substrate member (101), comprising: a first region (102) with a passive electrical component (104) with a first electrically conductive layer pattern (105) of an electrically conductive material and a second electrically conductive layer pattern (106) of an electrically conductive material deposited on respective sides (107, 108) of the semiconductor substrate member; wherein a trench (109) or through-hole (110) is formed (by etching) in the substrate within the first region, and wherein the electrically conductive material is deposited at least on a bottom portion of the trench or on a sidewall of the through-hole and electrically connected to one or both of the first conductive layer pattern (105) and the second conductive layer pattern (106); and a second region (103) with an active semiconductor component (111) integrated with the semiconductor substrate (101) by being fabricated by a semiconductor fabrication process. There is also provided a power supply, such as a DC-DC converter, embedded the semiconductor substrate member.

(fig. 1 should be published)


101
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107
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Fig. 1

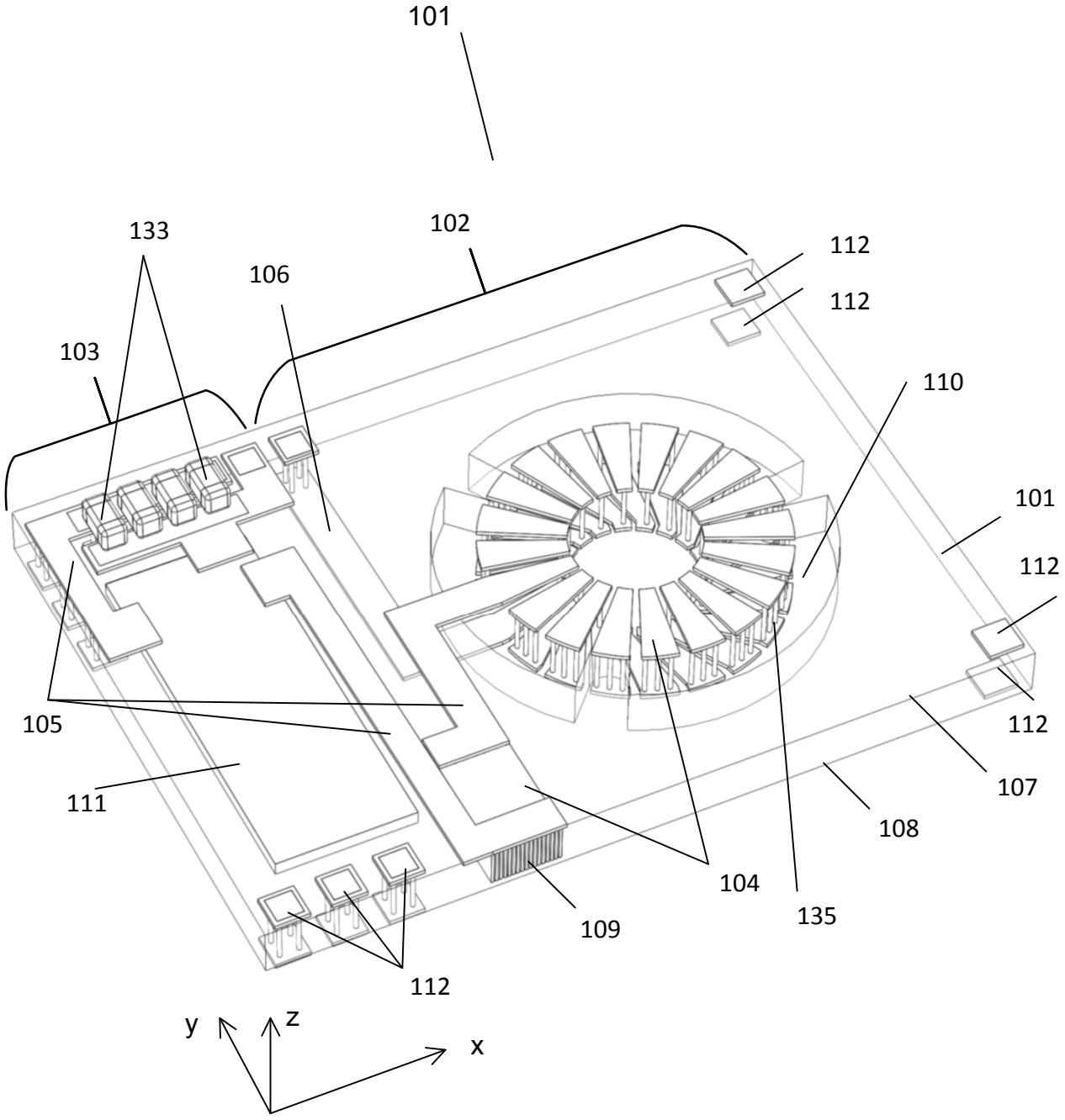
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Fig. 2

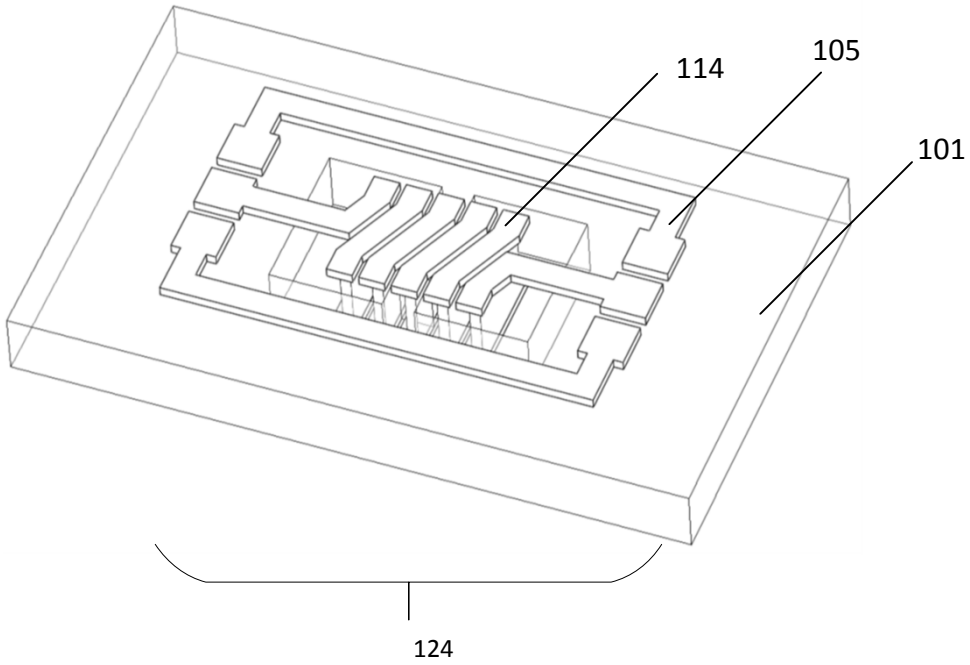


Fig. 3

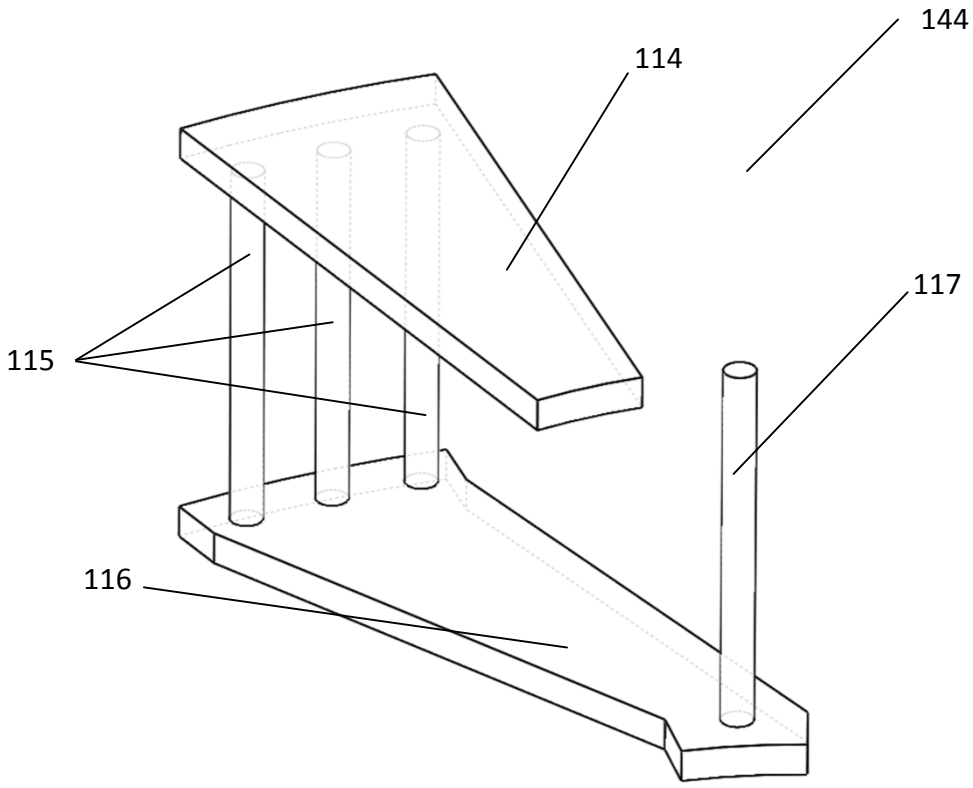


Fig. 4

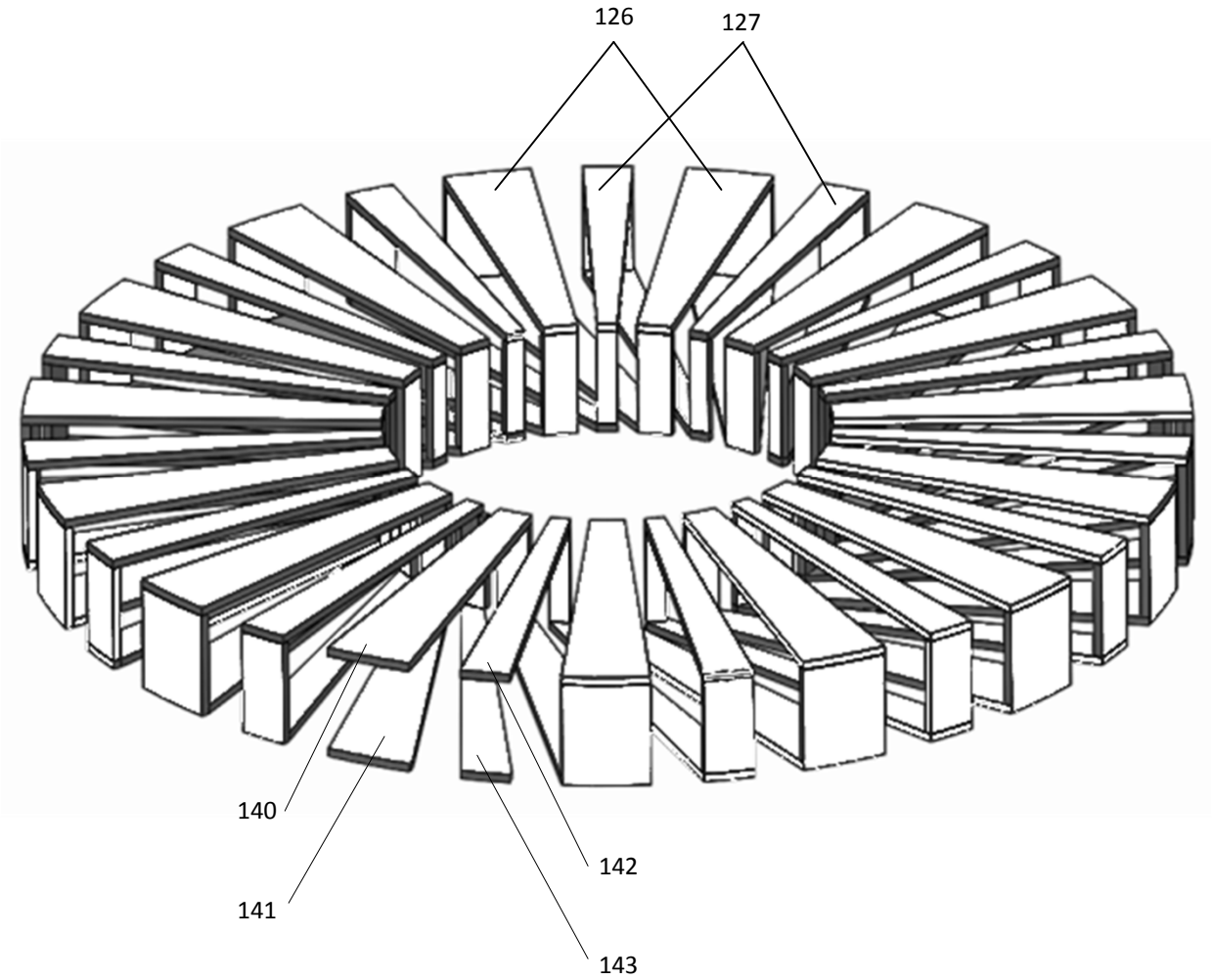


Fig. 5

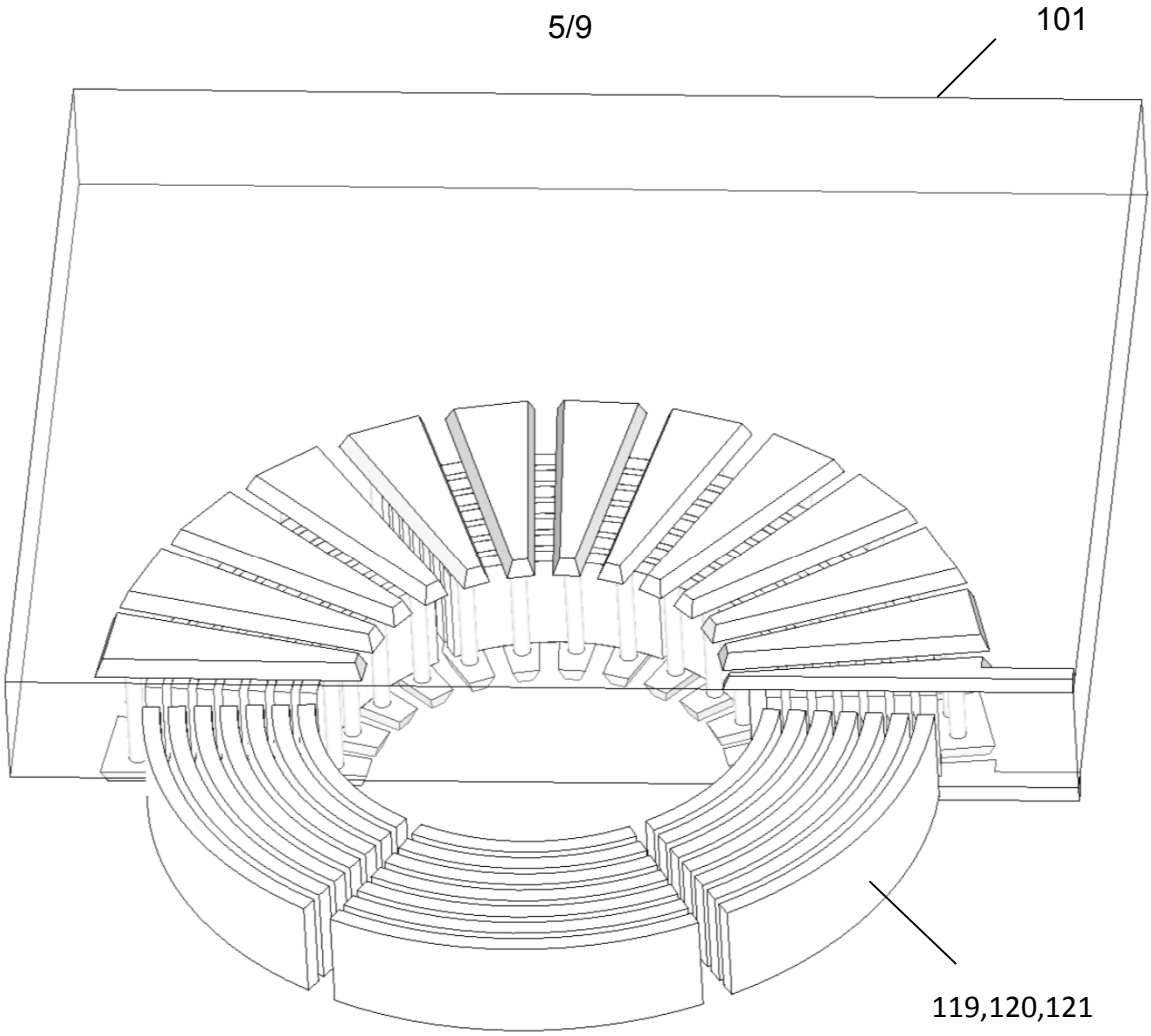


Fig. 6

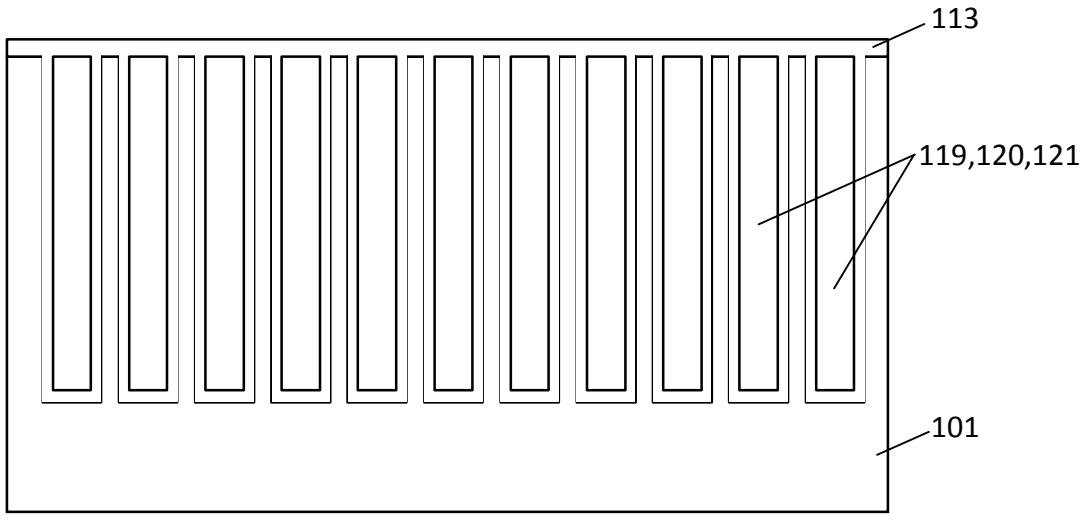


Fig. 7

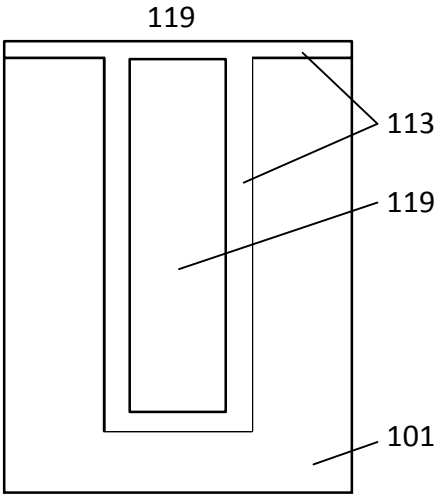


Fig. 8

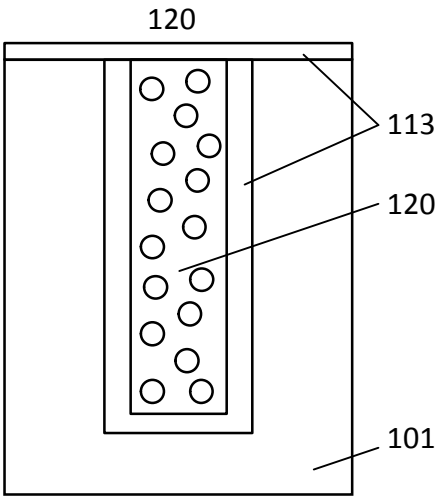


Fig. 9

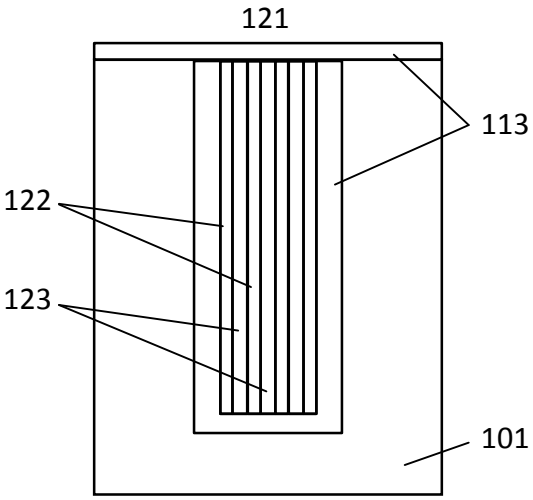
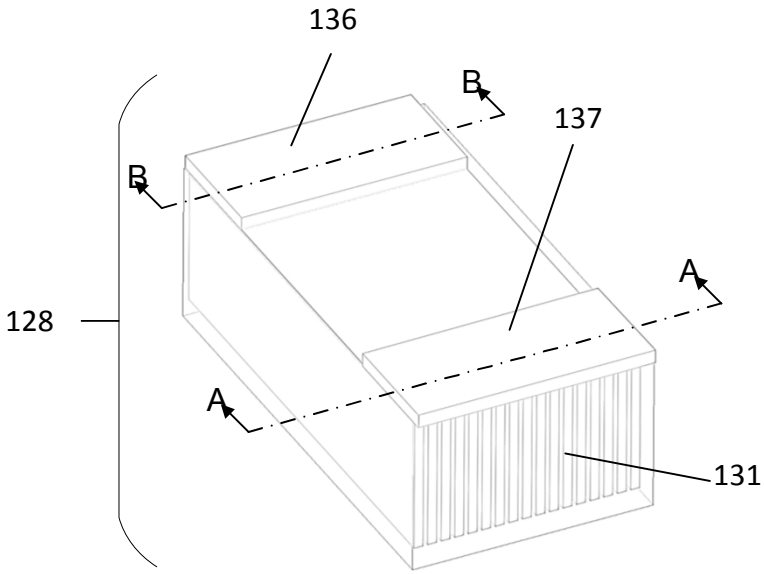
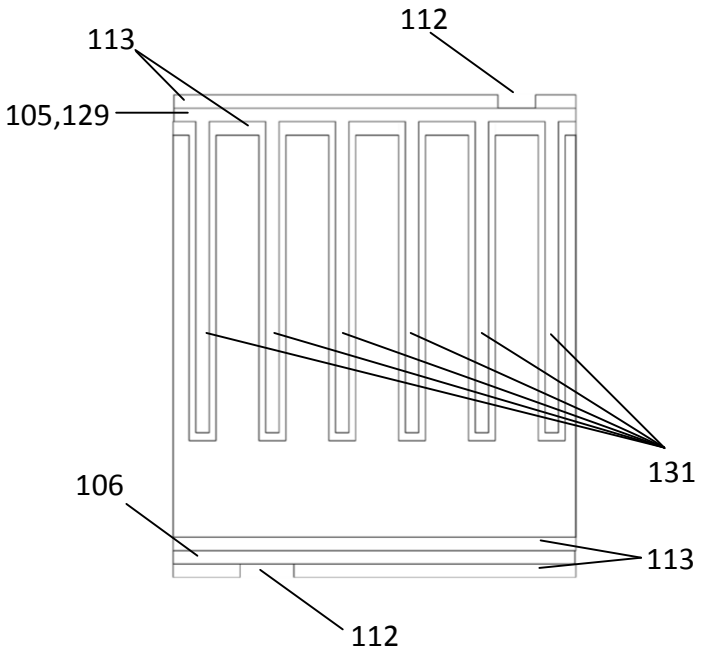
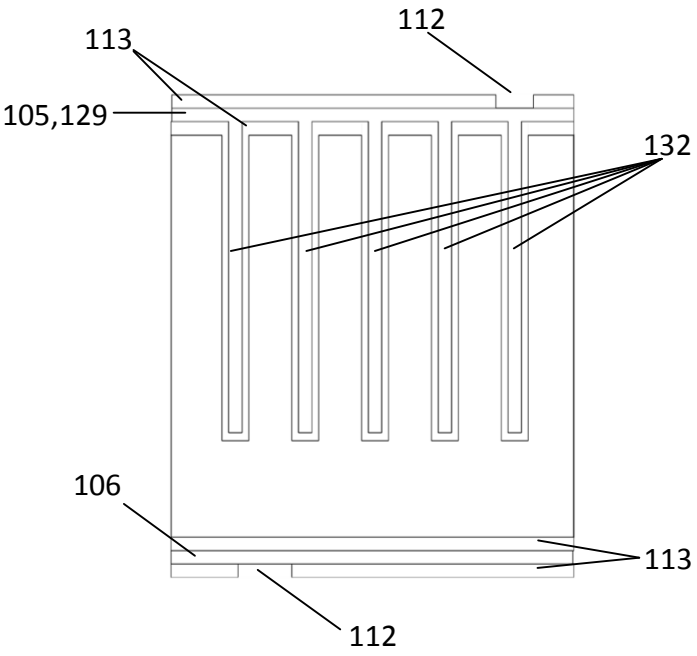


Fig. 10





Section A-A



Section B-B

Fig. 11

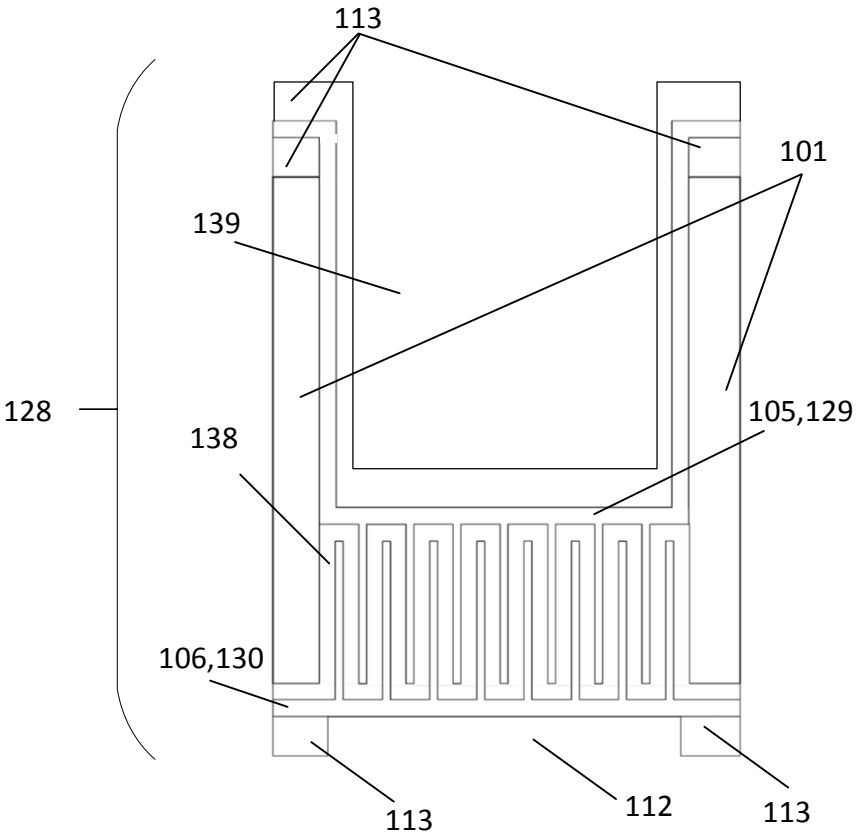


Fig. 12

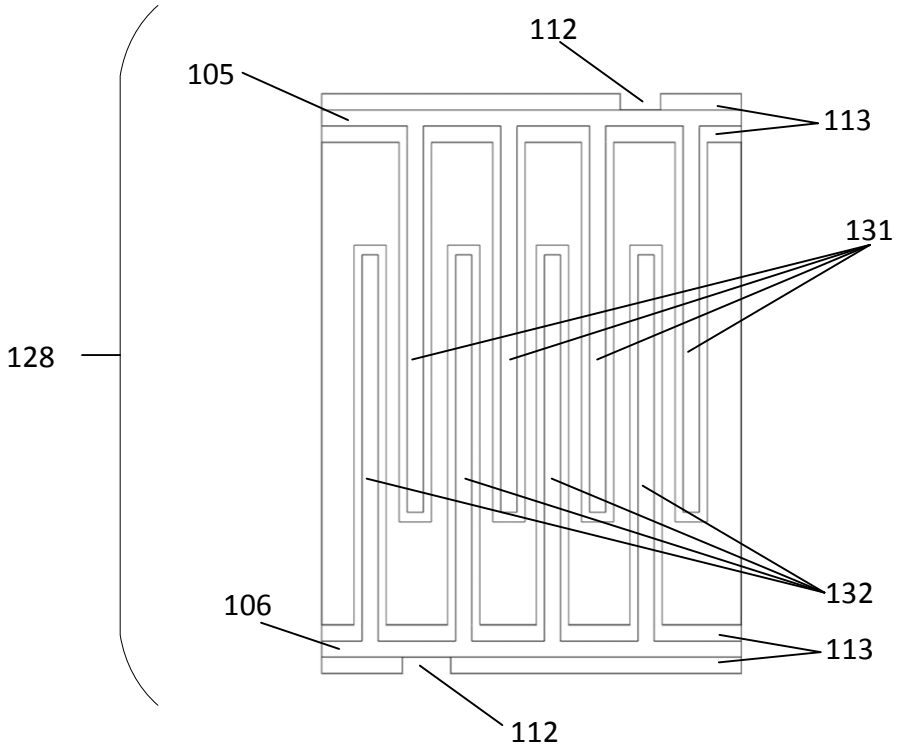


Fig. 13

Appendix A-J1

Hoà Thanh Le, Yasser Nour, Zoran Pavlovic, Cian O Mathuna, Flemming Jensen, Anpan Han, Santosh Kulkarni, Ziwei Ouyang, "High-Q 3D Microfabricated Magnetic-core Toroidal Inductors for Power Supplies in Package", submitted to IEEE Transactions on Power Electronics.

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High-Q 3D Microfabricated Magnetic-core Toroidal Inductors for Power Supplies in Package

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Keywords:	Inductors, Microelectromechanical devices, Power supplies

Note: The following files were submitted by the author for peer review, but cannot be converted to PDF. You must view these files (e.g. movies) online.

J3. Soft-core Inductor Fabrication.mov

High-Q 3D Microfabricated Magnetic-core Toroidal Inductors for Power Supplies in Package

Hoa Thanh Le, Yasser Nour, Zoran Pavlovic, Cian O Mathuna, Arnold Knott, Flemming Jensen, Anpan Han, Santosh Kulkarni*, Ziwei Ouyang*

***Abstract*— Integration of power inductors is a roadblock in realizing highly miniaturized power supply in package (PwrSiP) and power supply on chip (PwrSoC). Inductors in such power system are used for energy storage and filtering, but they dominate in size and loss. This paper presents a novel 3D in-silicon through-silicon via (TSV) magnetic-core toroidal inductor for PwrSiP. The magnetic powder based core is embedded into TSV air-core inductor using a casting method. The unique air-core inductor design with a hollow core and suspended windings enable a complete core filling with microscale magnetic powders. The proposed casting method is simple, scalable, and generic for a wide range of magnetic powders. TSV magnetic-core inductors are fabricated in a compact size of 2.4 x 2.4 x 0.28 mm with the core content varying from 63 to 88 weight percent of soft ferrite NiZn powders. The TSV magnetic-core toroidal inductors are fabricated and electrically characterized. Small-signal measurements show a three-fold higher inductance of 112 nH and a 30% higher quality factor of 14.3 at 12.5 MHz for magnetic core inductors compared to similar TSV air-core inductors. The small-signal measurement results are verified by the modelled results. The total core loss is characterized by large-signal measurements. A suitable inductor is implemented in a 12-MHz buck converter that operates in a zero-voltage-switching mode. The converter achieves a peak efficiency of 72% and the output power of 2.4 W converting 12 to 5 V_{DC}.**

***Index Terms*—Microfabrication, Inductor, through-silicon vias, PwrSiP,**

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I. INTRODUCTION

Miniaturization of power supplies are essential for the development of smart electronics systems e.g. internet of things (IoTs), light emitting diode (LED) lightings, and consumer electronic products [1]–[3]. As more functions are packed in a limited space in such electronic systems, power supplies are required to be more compact and efficient with a lower manufacture cost [4]–[6]. Monolithic integration of power supply system is known as power supply on chip (PwrSoC) solutions [5]–[10], in which all active and passive components are integrated on the same die, has been widely investigated as an ideal solution. However, a shorter-term solution is the power supply in package (PwrSiP) [5], [6] in which the discrete inductors and capacitors are packaged together with the power management integrated circuits. The evolution of such integrated power systems is highly correlated to the increase in the switching frequency i.e. $10-20$ MHz for co-packaged or stacked PwrSiP and to the very high frequency range ($30-300$ MHz) for PwrSoC [9]. High switching frequency enables the use of smaller inductors which often dominate in size and loss [4]–[6] allowing the integration of the inductors with other power components.

Microelectromechanical system (MEMS) technologies have showed a great potential for making compact, high-performance integrated inductors for a wide range of operation frequencies from a few MHz to the VHF range [8], [9]. The important advantage of MEMS inductors over the traditional discrete inductors is the possibility for IC integration and miniaturization. However, the integration of the magnetic core in the inductor structure is essential to achieve high inductance density and efficiencies. Another important aspect for PwrSoC and PwrSiP in which the active components are integrated in proximity to the inductors is the electromagnetic interference (EMI).

Toroidal inductors [11]–[14] are known for low EMI due to the high flux confinement. Other geometries, for example spiral inductors [15], [16], racetrack inductors [17], [18], and three-dimensional (3D) solutions such as solenoid inductors [19]–[21], often have strong out-of-plane stray fields. In addition, 3D toroidal inductors have a high inductance density and a high quality (Q) factor [22]. They are classified into on-silicon toroidal inductors [11], [23] and in-silicon toroidal inductors [14], [24]–[26]. While the fabrication technologies of on-silicon inductors are comparatively simpler in-silicon inductors have two important advantages in a smaller inductor height and the possibility for advanced packaging solution for PwrSiP and PwrSoC. As the windings are embedded in the Si substrate, the inductor height reduces which is an advantage for IC implementation [27]. Second, because in-silicon inductors are often fabricated with TSVs, these can be used as a passive interposer for co-packaged or stacked PwrSiP integration. Li

et al. [28] have demonstrated a PwrSiP using an interposer with a spiral inductor sandwiched between two magnetic sheets. This approach is a promising packaging technology for PwrSiP and PwrSoC, however, the limiting factor in size is the fabrication of dense TSVs.

Developing integrated inductors for PwrSiP often requires magnetic materials to achieve a useful inductance to operate at high-frequency range (10 - 20 MHz) [29]. Integration of the magnetic-core for the toroidal inductors is very challenging [26], [30]. Previous studies have reported on several deposition methods including electrodeposition, sputtering, and screen-printing, each of which has its own advantages and disadvantages as reviewed in [9]. Screen printing is a well-established and comparatively cheap technology that has been adopted for magnetic-core microinductors in the 1990s [31], [32]. The screen printing technique has the advantages of being a rather simple process with a wide range of printable materials, for example NiFe, NiFeCo for the KHz range, MnZn for frequencies below 5 MHz, and NiZn for an operating frequency as high as 10 MHz and above [28], [33]. NiZn is a preference due to its high resistivity and suitable relative permeability.

In this paper, we report a high-Q magnetic-core TSV MEMS toroidal inductors for high frequency (10 – 20 MHz) power conversions. Our process is fully compatible with the screen-printing technique for production scaling. This is demonstrated using a proof of concept casting process, where the magnetic material is embedded into the pre-fabricated MEMS Through Silicon Vias (TSV) air-core toroidal inductors reported in our previous work [34]. The concept is demonstrated using but not limited to a magnetic composite consisting of a non-conducting elastomer (PDMS) and 17-µm-diameter NiZn powders. The TSVs are fully filled with copper (Cu) to enhance the current handling capability which is tested up to 1.6 A. Adding the magnetic composite into the hollow air core improves significantly the electrical performance of the TSV inductors, i.e. 3 times higher inductance and 30% higher quality factor. The magnetic core also improves thermal dissipation and mechanical stability compared to the air-core inductors with suspended windings. A power converter with a switching frequency of 12 MHz was designed, and using its design specifications, a tailored TSV magnetic-core toroidal inductor is designed, fabricated, characterized, and implemented.

This paper is organized as follows: Section II presents the fabrication of the TSV magnetic-core toroidal inductor using a proof-of-concept casting process. Section III presents the magnetic characterization of the magnetic-core material and electrical characterization of the fabricated TSV inductors. The measurement results are compared to the

modelled results. Section IV describes the implementation of a 12-MHz buck converter using a TSV magnetic-core toroidal inductor and GaN FETs. The last section concludes the paper.

II. TSV Magnetic-core Toroidal Inductor

For the operational frequencies from 10 to 20 MHz, an inductance of 100s of *nH* is needed to achieve higher power converter efficiency and density. Magnetic core based inductors achieve significantly higher inductance densities in comparison to their air core equivalents, resulting in lower ripple current in the converter and lower losses. Fig. 1 shows the proposed TSV magnetic-core toroidal inductor fabricated based-on a pre-made TSV air-core inductor using a simple casting and curing process for the subsequent filling of the magnetic composite.

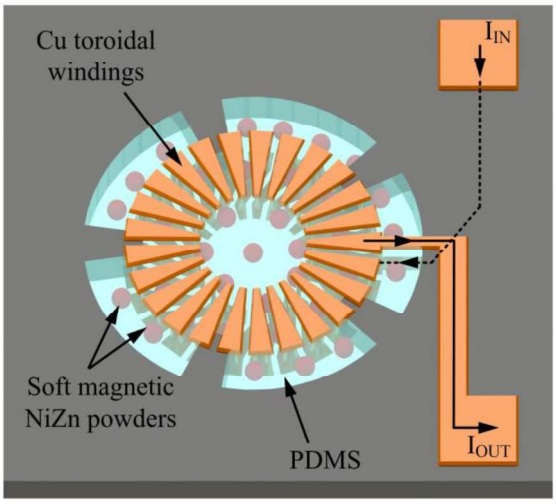

Fig. 1. A schematic of the TSV magnetic-core toroidal inductor fabricated with 50-µm-diameter TSVs, 50-µm-thick Cu windings, and an embedded magnetic core consisting of 17-µm-diameter soft magnetic NiZn powders mixed in a non-conducting polymer PDMS. The arrows illustrate the direction of the input current (I_{IN}) and output current (I_{OUT}).

The TSV air-core toroidal inductor is fabricated by a novel MEMS fabrication process reported in [34]. The process developed is based on MEMS fabrication technologies with the focus on CMOS compatibility, scalability, and flexibility. The process consists of 12 steps and 4 photomasks. The inductors used in this paper have 25 turns, the foot print is 5.5 mm^2, the TSV diameter is 50 µm, the inductor height is 250 µm, and the top and bottom conductors are 50-µm-thick.

Further, a composite magnetic core is filled into the hollow core of the TSV air-core toroidal inductor for making an isotropic toroidal core. The composite core consists of a polymer matrix material and soft-ferrite magnetic powders.

The polymer must be a non-conducting material with a low dielectric constant and a high resistivity to minimize parasitic capacitance and eddy-current losses. The soft ferrite powders must have low coercivity (H_c) for high-frequency operations, high resistivity (ρ) for low eddy-current losses, and the powder diameter has to be smaller than the inductor winding gap of 90 µm. Polydimethylsiloxane (PDMS) elastomer (Sylgard Rc 184, Dow Corning, USA) and FP350 (PPtechnology, USA) - fully-sintered soft ferrite NiZn powders are selected as the matrix polymer and the magnetic powders, respectively.

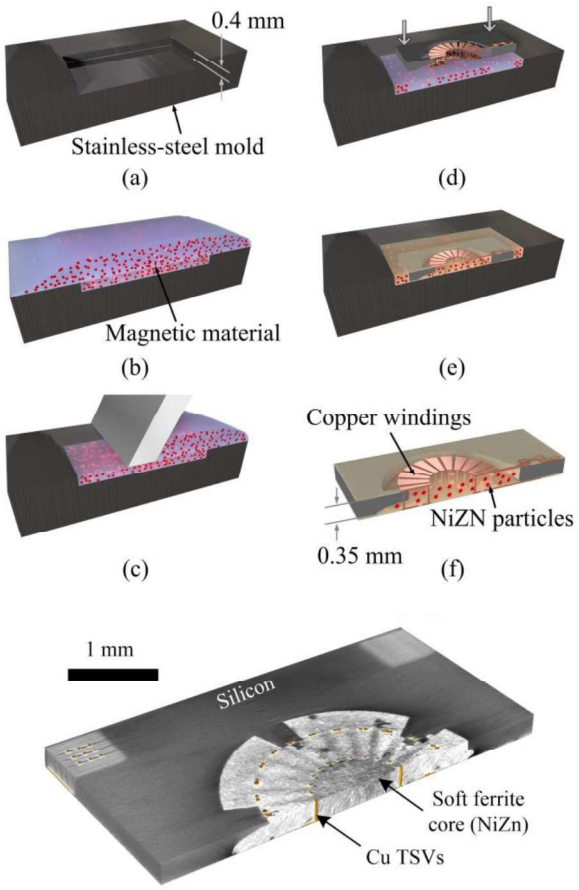

Fig. 2. A manual casting process for magnetic core fabrication. (a) Step 1: a stainless-steel mold with a 0.4-mm-deep, 6 x 6 mm cavity, (b) Step 2: casting of the composite material into the mold, (c) Step 3: a planarization step is done to get a uniform composite layer with a thickness of 0.4 mm. This is designed to be 50 µm higher than the inductor thickness of 350 µm to avoid overfilling of the core material over the copper windings. (d) Step 4: immerging of the air-core inductor into the composite layer, (e) Step 5: the core is cured at 75 °C for 3 hours, (f) Step 6: the inductor is released from the mold. (g) A cross-sectional micrograph

of a fabricated TSV magnetic-core toroidal inductor scanned by an X-ray inspection system XD7600NT (Nordson DAGE Corp., UK).

The fabrication process is described in Fig. 2 and animated in the Supplementary Video V1. A mixture of PDMS and FP350 NiZn ferrite powders are prepared and casted into a stainless-steel mold. The stainless-steel mold has two parts: a flat bottom plate and a top plate with a 5x5 mm, 400-µm-deep cavity. Two parts are attached together to create the mold in which the FP350-PDMS composite is printed (step 2, Fig. 2b). A planarization step is done to get the desired composite thickness of 400µm (step 3, Fig. 2c). An air-core toroidal inductor is immerged slowly into the mold until the top windings are covered. The sample is cured at 75 ^{o}C for 3 hours on a hot plate. The magnetic-core inductor is obtained after releasing from the mold (Step 6, Fig. 2f). Fig. 2g shows a cross-sectional micrograph of the fabricated TSV magnetic-core inductors scanned by an X-ray inspection system XD7600NT (Nordson DAGE Corp., UK). It is clearly shown that the magnetic core is fully filled without air-voids. In addition, it is noticed that the magnetic material covers the top and bottom windings thus confining the out-of-plan one-turn flux to further minimize the EMI issue.

The important parameters in the casting process are (i) a high-concentration core for a high inductance density, (ii) a homogeneous core with uniformly distributed magnetic powders for a good isolation between the powders, and (iii) a void-free filling without air gaps. In case of distributed air gaps, these will reduce the effective core volume thus reducing the effective permeability (μ_{eff}). In addition, they can create thermal instability due to the thermal expansion generated by the cycled temperature during operation. The casting process is optimized towards these objectives by varying the powder content (C_{FP350}). A high C_{FP350} increases the possibility of forming air gaps. Six inductors were fabricated with the C_{FP350} varies from 63 to 88 weight percent (wt%). The results are described in Table I and Fig. 3. At C_{FP350} = 88 wt%, big air avoids were observed as shown in Fig. 3b. The maximum C_{FP350} is 84 wt% for a void-free core as shown in Fig. 3c. Other factors are the curing temperature and curing pressure. A curing temperature was optimized at 75 ^{o}C.

The uniformity of the core depends on the size of the magnetic powders which must be smaller than the winding gap of 90 µm. Due to the limiting winding gap, it is required to perform a grinding step [35] for bigger powders or to use finer powders e.g. sub-micron or nanoscale powders [36]–[38]. The inductors made of finer powders will have higher packaging factors thus achieving higher inductance. The proposed process has an advantage in the flexibility to implement different magnetic materials and matrix polymers for other applications e.g. thermal conductive polymers

for better thermal dissipation. The proposed fabrication process was made on individual inductor dies but it can be scaled to the wafer-level processing by using a well-established screen-printing technique.

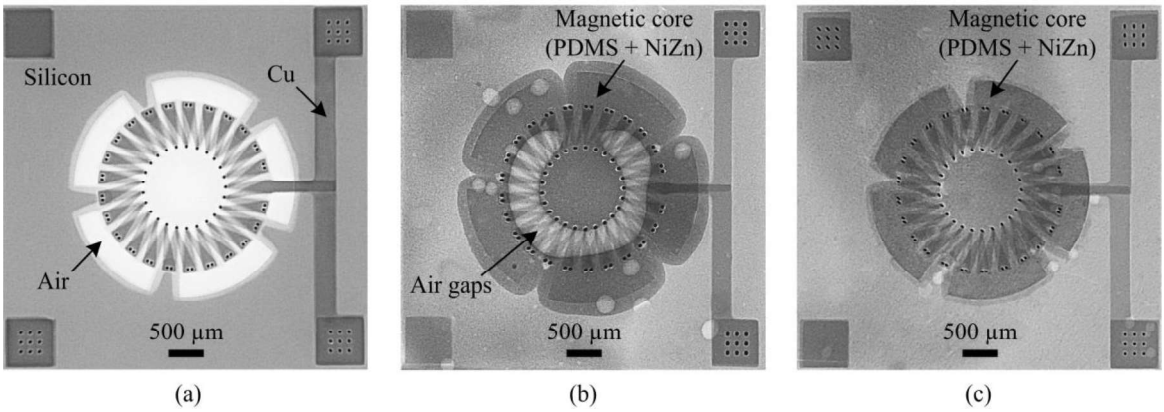

Fig. 3. X-ray micrographs of the fabricated TSV inductors. (a) A 25-turn, 350-µm-thick TSV air-core toroidal inductor. TSV magnetic-core inductors with the soft content C_{FP350} = (b) 88 wt% and (c) 84 wt%. The micrographs were captured by an X-ray inspection system XD7600NT.

TABLE I

OPTIMIZATION OF CORE CONCENTRATION

No.	FP350 (g)	PDMS (g)	Weight percent (wt%)	Effective μ_r	Fabrication results
1	1	0.5	63	2.3	Fully filled
2	1.5	0.5	71	2.4	Fully filled
3	2	0.5	77	2.5	Fully filled
4	2.5	0.5	81	2.7	Fully filled
5	3	0.5	83	3.0	Fully filled
6	3.8	0.5	89	-	Big air gaps

III. ELECTRICAL CHARACTERIZATION

A. Small Signal Measurement

The TSV air-core and magnetic-core toroidal inductors were electrically characterized using a precision impedance analyzer and vector network analyzer (VNA). The two-port scattering-parameters were measured on a E5071C VNA (0.3 MHz – 20 GHz, Agilent, USA) with 500-µm-pitch ground-signal (GS) probes connected to two terminals of the

inductors as shown in Fig. 1a. The measured S-matrix was then converted to the Z-matrix which is used to extract the inductor's equivalent elements i.e. resistance and inductance. The bias measurements were done by using a HP4285 LCR meter and a current source HP42841.

Fig. 4 presents the small-signal measurement results of the air-core and magnetic-core TSV toroidal inductors. The inductances measured at 1 MHz of the air-core and magnetic-core inductor are 38.2 nH and 86.0 nH, respectively. The calculated inductances using equation (1), are 37.5 nH (air core) and 85.2 nH (magnetic core). Several models for the TSV air-core toroidal inductor are presented in [22], [39]–[41]. A parasitic capacitance model is presented in [40]. The air-core inductance is calculated by eq (1) with two terms created by an N-turn poloidal current and a single-turn toroidal current, respectively. From 1 to 50 MHz, this model has less than 6.7 % error compared to the measured air-core inductance. The inductance of the TSV magnetic-core toroidal inductor (L_{mag}) is calculated using a relative permeability μ_r =2.4 which is measured by a high-frequency permeameter (PMM-9G1; Ryowa Electronics Co., Ltd., Japan). It is assumed that in the frequency range below 50 MHz, the permeability is frequency-independent. In Fig. 4a, L decreases slightly with frequency resulting in a slight inductance drop of 4 % at frequencies above 40 MHz. On the other hand, the modelled inductance, which is calculated as the imaginary part of the inductor impedance, increases slightly at the frequency above 40 MHz due to a resonant effect with the measured resonant frequency of 142 MHz. The inductance model for L_{mag} has less than 5.5 % error for the TSV magnetic-core toroidal inductor:

$$\mathrm{L} = \mu_r \left[\frac{N^2 h \mu_o}{2\pi} ln\left(\frac{R_o}{R_i}\right) + \frac{R_o + R_i}{2} \mu_o \left[ln\left(8 \cdot \frac{R_o + R_i}{R_o - R_i}\right) - 2 \right] \right] \quad (1)$$

where N is the number of turns, h is the inductor height, μ_r is the relative permeability of the core material, R_i and R_o is the inner and outer radius of the TSV toroidal inductor.

Fig. 4b shows the measured and calculated AC resistance (R_{small}) of the TSV air-core and magnetic-core inductors. In this model, it is assumed that the current in the TSVs, top and bottom conductors flows in a skin depth facing the high-field inner region of the toroidal core. The TSV air-core inductor has a resistance of 0.26 Ω at 1 MHz and 0.40 Ω at 12.5 MHz. The calculated resistances are 0.25 Ω and 0.38 Ω at 1 MHz and 12.5 MHz, respectively. For the air-core, the model has an error less than 10 % for frequencies up to 25 MHz. The magnetic-core inductor has a higher resistance with 0.27 Ω at 1 MHz and 0.49 Ω at 13 MHz. The small-signal resistance (R_{small}) is modelled with a winding resistance and an equivalent eddy-current-loss resistance. The winding resistance includes TSVs resistance (R_{via}) and slab

resistance (R_{slab}) which are calculated by eq (2) [40] and (3), respectively. The trapezoidal wet-etched profile of the top and bottom windings is accounted in eq (3).

$$R_{Via} = \frac{\mathrm{N}\rho h}{2\delta(d_{via} - \delta)}\left(\frac{1}{n_i} + \frac{1}{n_o}\right) \tag{2}$$

$$R_{slab\_top} = R_{slab\_bot} = N\rho \int_0^l \frac{1}{\delta[2\pi(R_i + x)/N - G_W - 2\,\delta(f)/\tan(2\pi/N)]}\,dx \tag{3}$$

where n_i and n_o are the number of the inner and outer TSVs. ρ is the conductivity of the winding material and $\delta = \sqrt{1/\pi f \mu\sigma}$ is the skin depth where f is frequency, μ is copper permeability ($4\pi 10^{-7}$ H/m), and σ is copper conductivity. h is the wafer thickness and d_{via} = 50 μm is the diameter of the TSVs. The top and bottom slab resistances are calculated using the same eq (3) by replacing the slab length (l) by the top slab length (l_{top}) and the bottom slab length (l_{bot}). l_{top} and l_{bot} are calculated by the eqs. (4) and (5), respectively. G_w = 90 μm is the winding gap.

$$l_{top} = R_o - R_i \tag{4}$$

$$l_{bot} = \sqrt{{R_o}^2 + {R_i}^2 - 2(R_o - R_i)R_i \mathrm{Cos}(2\pi/N)} \tag{5}$$

It is noted that the Q model is less accurate at frequencies above 20 MHz with more than 11 % error. This is because the modelled resistance is lower than the measured resistance. The resistance model does not account for the proximity effect between the winding slabs and TSVs. An additional contribution to the resistance is a high current density at the connections between TSVs and the perpendicular winding slabs. This effect is not considered in the resistance model.

As shown in Fig. 4a, the TSV magnetic-core inductor has a peak Q of 14.3 measured at 12.5 MHz as compared to a peak Q of 10.3 at 47 MHz of the air-core inductor. The increased Q for the magnetic core device is due to the higher inductance and lower eddy current losses in the core material at lower frequencies. On increasing frequencies, the eddy current losses in core increase, reducing the inductance and hence the Q-factor. The inductances measured at 1 MHz of the air-core and magnetic-core inductor are 38.2 nH and 86.0 nH, respectively.

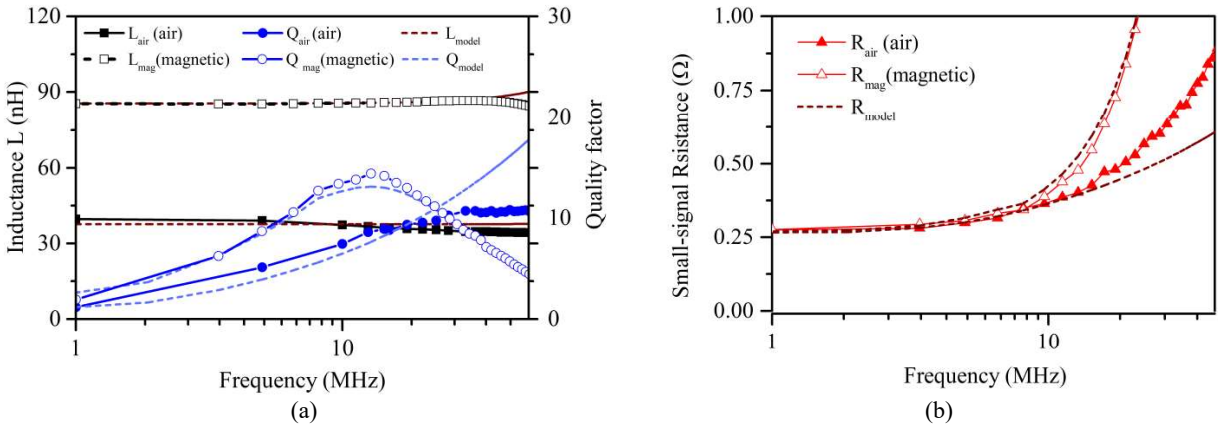

Fig. 4. Small signal measurement and the modeling results of the TSV inductors. (a) Measured inductance of the air-core (L_{air}) and magnetic-core (L_{mag}) TSV inductors and the quality factor of the air-core (Q_{air}) and the magnetic-core (Q_{mag}) TSV inductors. The magnetic -core inductor has a higher peak Q of 14.3 at 12.5 MHz compared to the peak Q of 10.7 at 47 MHz. (b) The measured resistance of the TSV air-core (R_{air}) and magnetic-core (R_{mag}) inductors. The discontinuous lines show the calculation results.

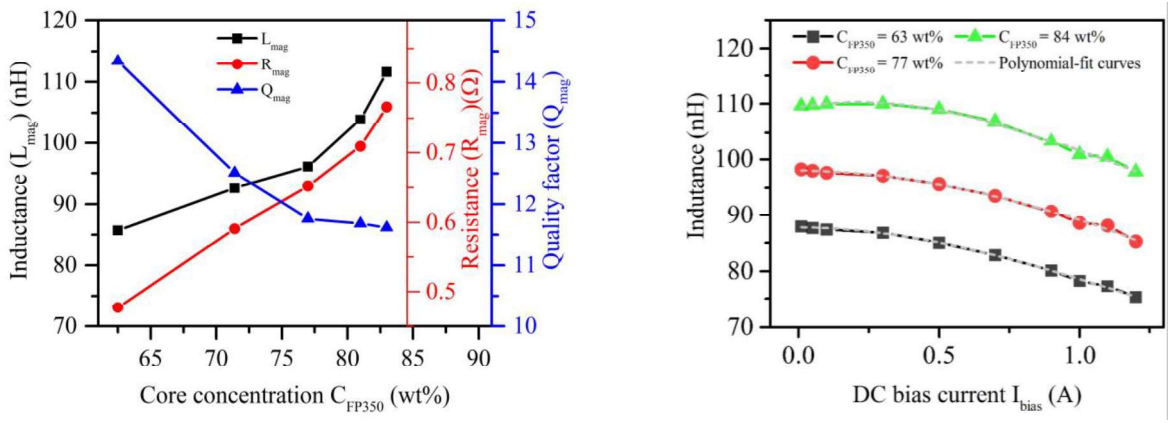

Fig. 5. (a) Measured small-signal L_{mag}, R_{mag}, Q_{mag} as a function of core content C_{FP350} measured at 12.5 MHz. (b) L_{mag} versus bias current (I_{bias}) from 0A to 1.2A. The dashed lines are 3rd-order polynomial fitting curves. A saturation current of 1.6 A is estimated with a 20 % drop of inductance.

Fig. 5a shows the measured L_{mag}, R_{mag}, and Q_{mag} of the TSV magnetic-core inductors fabricated with a core concentration (C_{FP350}) from 63 wt% to 84 wt%. The measurements were operated at 12.5 MHz. As expected, L_{mag} increases from 86 nH to 112 nH for C_{FP350} from 63 wt% to 84 wt%. R_{mag} increases with higher C_{FP350} due to an increased eddy-current loss in larger soft-ferrite volumes. This results in a decrease of Q_{mag} from 14.3 to 11.5. Even though adding the magnetic core improves the Q factor by 30 % compared to that of the air-core inductor, the peak Q still decreases with an increasing C_{FP350}. Adding more core material introduces more core eddy-current losses in the device

which has a higher frequency dependency than copper eddy current losses. In addition, because the winding resistance is altered by the strong magnetic field generated in the magnetic core, adding more core material will affect the current density and hence the winding resistance.

Furthermore, the fabricated TSV magnetic-core inductors were characterized under a DC bias current (I_{DC}) from 0 to 1.2 A as shown in Fig. 5b. All tested inductors showed a similar inductance drop of 14.1 % (at I_{DC} = 1.2 A) from its initial inductance (at I_{DC} = 0 A). This drop is due to the saturation response of the soft magnetic materials to the applied field, hence the effective core volume reduces gradually. This reduction results in a lower effective permeability of the core thus reducing the inductance. As the bias current increases, the core is gradually saturated and thus the inductance decreases. The saturation current (I_{sat}), which is defined by a 20 % drop in inductance, is estimated to be 1.7 A from the extrapolating 3rd-order polynomial fitting curve.

Table II compares the small-signal performance of the fabricated TSV magnetic-core inductors to the prior art of MEMS power inductors. The demonstrated TSV inductors (this study) have a higher Q factor than most of the integrated inductors reported in [9] and in Table II while the inductance and DC resistance are in the same range. The TSV toroidal inductors occupy a footprint of 2.4 x 2.4 mm and a height of 0.28 mm. The proposed inductors are evaluated and compared using a figure of merit (FOM) which is calculated by $FOM = \sqrt{Q_{DC} \cdot Q_{AC}}/V$, where $Q_{DC} = L_{DC}/R_{DC}$, Q_{AC} is the peak small-signal Q, and V is the volume of the fabricated inductor including the substrate thickness for our inductors. The fabricated TSV magnetic-core toroidal inductors have a higher FOM than most of the reported inductors. The FOM employed here includes both the dc and ac performance of the device, which in most cases are inversely dependent. For example devices which achieve higher inductance densities (solenoid) with increased windings, typically have higher Q_{AC}, but suffer from higher DC resistance. Similarly, devices achieving higher inductance densities with increase magnetic core contribution (stripline) have improved dc losses in comparison to their ac performance. Hence, a FOM where both these factors are considered presents a more realistic comparison between the different devices. One factor still not included in the FOM is the current handling capability of the device, as this data is not widely reported, the authors have chosen to use the FOM metric described above in this study.

The performance of the TSV inductors can be improved further by optimizing the winding design, for example smaller winding gaps for higher winding density and larger and denser parallel TSVs for lower winding resistance. Alternative advanced magnetic materials e.g. iron-based nanocrystalline materials [36]–[38] with high saturation and

high permeability can be used to enhance the inductance and power density. The magnetic materials have to be pre-sintered to avoid a high-temperature sintering process which is incompatible with CMOS fabrication technologies.

TABLE II

SMALL-SIGNAL PERFORMANCE OF THE TSV MAGNETIC-CORE TOROIDAL INDUCTOR COMPARED TO THE PRIOR WORKS

Study	Inductor	Core	L (nH)	Q_{max} @ f (MHz)	R_{DC} (mΩ)	I_{sat} (A)	Footprint (mm^2)	Height (mm)	Figure of Merit (FOM) $\sqrt{Q_{DC} \cdot Q_{AC}}/V$
This study	**In-Si 3D toroid**	**NiZn + PDMS**	**85**	**14.3 @ 12.5**	**230**	**1.6**	**5.6**	**0.35**	**1.21**
	In-Si 3D toroid	**NiZn + PDMS**	**112**	**11.5 @ 12.5**	**265**	**1.6**	**5.6**	**0.35**	**1.15**
UF [35]	In-Si 2D spiral	NiZn + PDMS	390	10 @ 6	140	-	9	0.83	0.71
UF [24]	In-Si 3D toroid	NiZn + PDMS	160	10.5 @ 14	265	-	169	0.32	0.05
HKUST [25]	In-Si 3D toroid	MnZn + PDMS	43.6	16.2 @ 65	280	-	2.9	-	-
Gatech [14]	In-Si 3D toroid	Air	60	17.5 @ 70	191	-	36	0.6	0.11
Gatech [26]	In-Si 3D toroid	CoNiFe	1000	18 @ 1	700	-	100	1	0.05

UF: University of Florida, USA; HKUST: Hong Kong University of Science and Technology, Hong Kong; Gatech: Georgia Institute of Technology, USA.

However, small-signal measurements are not sufficient to evaluate the magnetic-core inductor due to the different loss mechanisms in the core, including hysteresis loss and anomalous loss which only appear at large ac currents. Characterization and testing of the magnetic-core inductors in large-signal condition (i.e. large amplitude AC signal or in power converter) is discussed in the next section.

B. Large Signal Measurement

The large-signal losses of the TSV magnetic-core inductor was measured in the frequency range from 10 to 15 MHz. The measurement setup consists of two blocks: the signal generation system and the measurement system. The signal generation system generates a sinusoidal excitation current with a high-amplitude, high-frequency AC current along with a DC bias current. The AC current is generated by a signal generator E8257D (250 KHz – 20 GHz, Agilent, USA) and then amplified by an RF-amplifier model 25A250A (10 kHz - 250 MHz, Amplifier Research, USA). A DC bias current is generated by a bench top power supply 72-10480 (3A, TENMA, Japan). The voltage and current across the inductor are sensed by 1.5 GHz active probes (Tektronix, USA) and recorded by a mixed domain oscilloscope

MDO3104 (Tektronix, USA). The details of the measurement technique including current sensing and compensation are reported in [42].

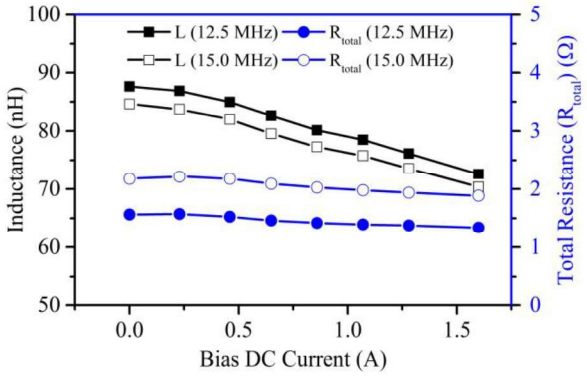

Fig. 6. The large-signal inductance and resistance (R_{total}) of a 63-wt% TSV magnetic-core inductor with a 200-mA peak-to-peak AC current and DC currents (0 – 1.6 A).

Fig. 6 shows the large-signal testing results of a 63-wt% TSV magnetic-core toroidal inductor. The inductance and total resistance (R_{total}) were measured with a DC bias current from 0 to 1.6 A and a 12.5 MHz, 0.2 A AC current. The inductance drops 17 % at bias current of 1.6 A giving an estimated saturation current of 1.7 A. R_{total} increases from 1 to 2 Ω as the frequency increase from 10 to 15 MHz. R_{total} includes all core losses including the hysteresis loss and the anomalous loss which are neglected in small-signal measurement due to smaller excitation AC currents. The measured R_{total} is shown in Fig. 6. It is noted that R_{total} drops from 1.48 Ω to 1.35 Ω with an increased bias current from 0 to 1.6 A. This can be explained by the fact that when some portion of the core enters saturation, the effective core volume reduces. The saturated core volume does not contribute to the inductance but also does not add to the losses. Hence, increasing the DC current leads to a lower inductance and a lower AC core resistance.

Fig. 7 show the core loss separation from the large-signal testing of 63-wt% TSV magnetic-core inductor. The total loss (P_{total}) consists of four losses including eddy-current core loss and winding loss ($P_e + P_w$),hysteresis loss (P_h), and anomalous loss (P_a). P_{total} is calculated from the large-signal resistance by $P_{total} = R_{total}.I_{acrms}^2$. It is interesting to note, as the test frequency is increased from 10 MHz to15 MHz, the contribution of $P_e + P_w$ decreases from 49% to 35 % of the total loss. Assuming that the magnetic core does not significantly alter the current density in the copper windings, the winding resistance is the same for the TSV air-core and magnetic-core toroidal inductors. Hence, by subtracting the air-core resistance, the increased resistance is due to the added magnetic core. This increased resistance results in an additional core loss which is considered as the eddy-current loss (P_e). P_e contributes an average proportion of 13.6 ±

0.15 % to P_{total} at the frequency from 10 to 15 MHz. This is because the magnetic powders have high resistivity and they are isolated with high-resistivity PDMS.

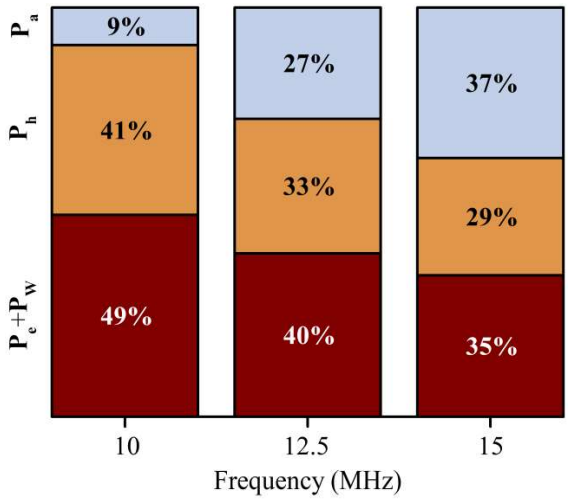

Fig. 7. Core loss separation of a 63 wt% TSV magnetic-core toroidal inductor based on large-signal measurements. The winding loss and eddy-current loss ($P_w + P_e$) from small signal measurement, the hysteresis loss (P_h), and the anomalous loss (P_a) are shown in the percentage measured from 10 to 15 MHz

The core loss is analyzed as follows: The eddy-current loss in powder-core inductor is empirically modelled by the model developed by Skarrie [43] The measured small-signal resistance as the experimental data to determine the eddy-current loss coefficient. A similar method was reported in [44]. The hysteresis loss is modelled using (6) [45], and the anomalous loss, which is the subtraction of the total loss to the other losses, is calculated by $P_a = P_{total} - P_e - P_h$.

$$P_h = 4 f {B_{ac}}^2 \frac{H_c}{B_{sat}} \tag{6}$$

where f is the excitation frequency, B_{sat} is the saturation magnetic flux density, B_{ac} is the applied AC flux density, and H_c is the coercivity.

The proportion of the hysteresis loss is therefore corresponding to 41 % and 29 % the total core loss at 10 and 15 MHz. The anomalous loss, which is the subtraction of the total loss to the other losses, is calculated by $P_a = P_{total} - P_e - P_h$. It is noted that the anomalous loss contributes 9% and 37% of the total loss at 10 MHz and 15 MHz, respectively. The loss mechanism of the anomalous loss is often explained as excess eddy-currents which appear along the ferrite grain boundaries when subjected to fast switching, large ac fields. This is different to traditional eddy currents which

are a macroscopic loss, primarily frequency-dependent phenomena and appear within the material to oppose flow of flux. The anomalous losses are dependent both on frequency and amplitude of applied ac fields.

From the calculated losses, equivalent resistances for the core loss can be calculated to build an equivalent model of the TSV magnetic-core toroidal inductor (Fig. 8) which can be used for inductor design.

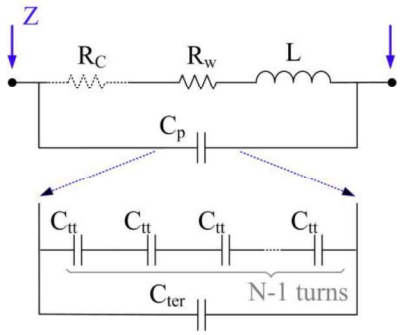

Fig. 8. An equivalent model of the complex impedance (Z) of the TSV air-core toroidal inductor with a winding resistance (R_w), an ideal inductance (L), and a winding capacitance (C_p). An equivalent core resistance (R_c) representing the total core loss is added to model the TSV magnetic-core toroidal inductor. C_p includes a terminal capacitance (C_{ter}) between inductor input and output and N – 1 turn-to-turn capacitance (C_{tt}) connected in serial.

IV. 12 MHz Buck Converter

A high frequency soft-switching buck converter was designed and implemented using an 85-nH TSV magnetic-core toroidal inductor and gallium nitride (GaN) field effect transistors (FETs). A schematic of the converter's power stage is shown in Fig. 9a. The converter consists of two EPC8004 40 V GaN FETs (Q_{HS} and Q_{LS}) driven by a LM5113 high speed gate driver, a TSV magnetic-core toroidal inductor (L), input capacitors (C_{IN}) and output capacitors (C_{OUT}). The power stage is driven by a tunable pulse width modulator with an adjustable dead time capability. A summary of the designed voltage regulator components is shown in Table III.

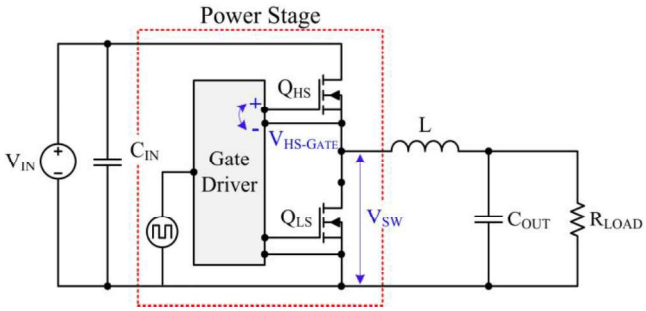

Fig. 9: A schematic of a buck converter using two 40-V GaN FETs and a TSV magnetic-core inductor.

TABLE III

TESTING SPECIFICATION FOR A BUCK CONVERTER

Parameter	Value	Description
V_{IN}	12 V	Input Voltage
V_{OUT}	3.3 – 5 V	Output Voltage
I_{OUT}	0 – 0.5 A	Output Current
f_{SW}	12 MHz	Switching Frequency
L	85 nH	Inductance

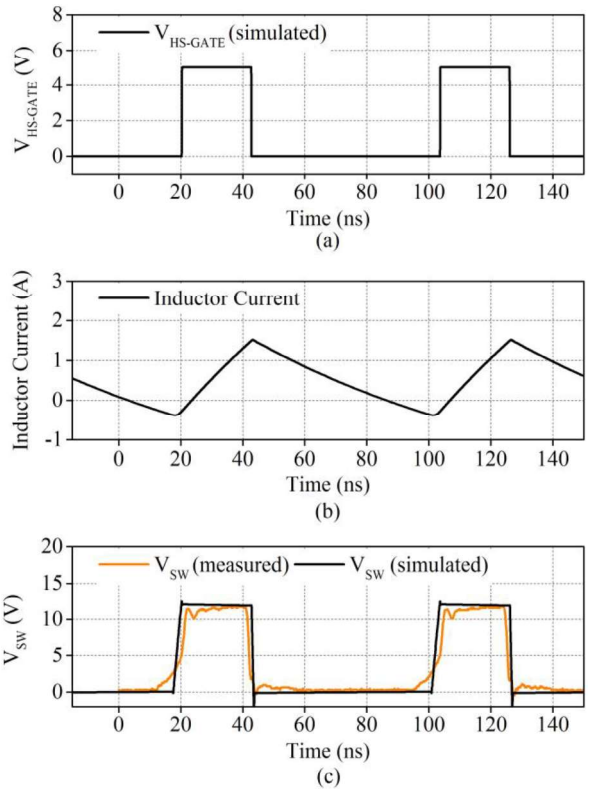

Fig. 10: (a) Simulated waveform of the high-side gate voltage ($V_{HS-GATE}$), (b) Simulated waveform of the inductor current, (c) Simulated and measured waveforms of the switching voltage (V_{SW}).

The detailed operation of such zero-voltage switching (ZVS) converter using an air-core spiral inductor is reported in [46]. The converter along with the TSV inductor is simulated using LT-spice. The simulation model for the inductor was built based on the small-signal and large-signal measurements to account for the winding loss and the core losses. Fig. 10 presents the simulated and measured waveforms. Fig. 10a shows the simulated waveforms of the high-side gate voltage with 3.3 V output voltage. The switching voltage (V_{SW}) waveforms verify that the converter is operating in

ZVS mode. Fig. 10b shows the simulated inductor current which consists of a 0.5 A DC current and a 0.84 A RMS AC current. The measured waveform at the switching node is shown in Fig. 10c which indicates that the converter operates in ZVS when the FETs are turning ON. It is also noted from the measured waveform that the converter is partially soft switching due to the probe capacitance loading effect. Fig. 11 presents the efficiency (η) and output power (P_{out}) as a function of the output current (I_{out}) from 0 to 0.5 A for two output voltages of 3.3 V and 5 V. The converter achieves a peak efficiency of 71.6 % at V_{out} = 5 V and P_{out} = 2.4 W.

The power loss of the TSV magnetic-core toroidal inductor in the converter is determined by the thermal measurement method [47] via DC power loss. The power loss is 0.63 W and 0.79 W for V_{out} of 3.3V and 5 V, respectively. Fig. 12 shows the thermal images of the inductor under the AC power loss in the converter (Fig. 12 a, b) and the DC power loss (Fig. 12 c, d). It is noted that in the magnetic-core inductor, the heat is dissipated more uniformly through the magnetic core confirming the advantage of the magnetic core for better heat transfer. The thermal performance could be further improved by replacing PDMS by a thermal epoxy e.g. EPO-TEK® 921-FL (Epotek, USA has thermal conductivity = 1.1 W/mK, and high resistivity > 6. 10^{11} Ωm).

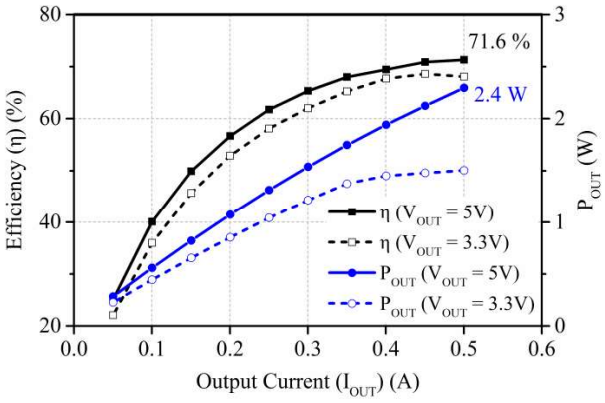

Fig. 11: The measured efficiency (η) and output power (P_{out}) with the output current (I_{OUT}) from 0 to 0.5 A. The output voltage (V_{OUT}) is 3.3 V and 5 V. A peak η of 71.6 % and a maximum P_{out} of 2.4 W was achieved at V_{OUT} = 5 V.

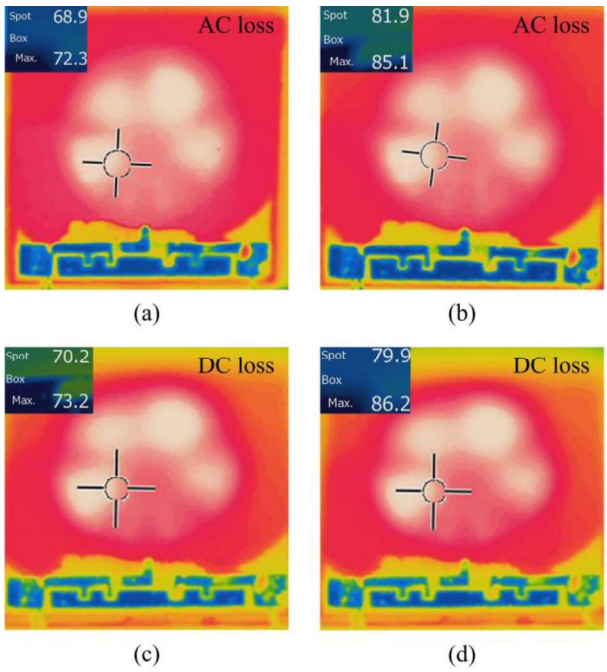

Fig. 12: Thermal image of a TSV magnetic-core inductor in the converter at I_{OUT} = 0.5 A with the output voltage of (a) V_{out} = 3.3 V, (b) V_{out} = 5.0 V. A thermal image of the inductor under a DC power loss of (c) 0.63 W (V_{DC} = 0.56 V, I_{DC} = 1.11 A) and (d) 0.79 W (V_{DC} = 0.65 V, I_{DC} = 1.23 A). The DC power loss in the inductor is 0.63 W and 0.79 W for V_{out} of 3.3 V and 5V, respectively.

V. Conclusion

A high-Q TSV magnetic-core toroidal inductor for high frequency (10 – 20 MHz) power conversions has been reported. The TSV magnetic-core toroidal inductors were modelled, fabricated, characterized and tested in a high-frequency converter. The fabricated TSV NiZn-core toroidal inductors have a peak Q factor of 14.3 and an inductance of 85 – 112 nH. A selected inductor was used to implement a 12-MHz ZVS buck converter which achieved a peak efficiency of 72 % and successfully delivered 2.4 W to the output at the input voltage of 12 V and the output voltage of 3.3 V and 5 V. The magnetic core was integrated using a simple casting process with the potential of printing a wide range of microscale magnetic powders for other applications. Furthermore, using TSVs to build the in-Si inductor could enable the fabrication of passive interposers with integrated 3D inductors for PwrSiP and potentially for PwrSoC integration.

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Appendix A-J2

Jens Christian Hertel, Yasser Nour and Arnold Knott, "Integrated Very High Frequency Switch Mode Power Supplies: Design Considerations," in IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE), 2017.

Integrated Very High Frequency Switch Mode Power Supplies: Design Considerations

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Integrated Very High Frequency Switch Mode Power Supplies: Design Considerations

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***Abstract*—This paper presents a power supply using an increased switching frequency to minimize the size of energy storing components, thereby addressing the demands for increased power densities in power supplies. 100 MHz and higher switching frequencies have been used in resonant power converters, which along with the possible integration of passive components on silicon wafer, present a beneficial solution in applications such as mobile phones. This paper presents a design for a 9 W class E resonant power converter in an 0.18 μm CMOS process. The converter is driven by a self oscillating gate drive, which is presented in an in-depth mathematical analysis. The gate resistance of the designed transistors is of critical importance in order to achieve the correct phase shift required for zero-voltage-switching. The Z-parameter method is used to characterize the transistors which is verified through simulations. The required spiral inductors was modeled, and simulations show Q values of as high as 14 at a switching frequency of 250 MHz. Simulations of the converter show an efficiency of 55 % with a self oscillating gate drive. However the modeled inductor was not adequate for operating with the self oscillating gate drive, presenting a future challenge for power supplies on chip.**

***Index Terms*—DC-DC power converters, Radiofrequency integrated circuits, VHF circuits, Integrated circuit modeling, Zero voltage switching**

I. Introduction

Consumer, industrial and automotive electronics are ever decreasing in size and consequently, the demand for smaller power supplies is increasing. The size of power supplies can be reduced through increasing the switching frequency, minimizing the energy storing components. In the classic hard-switched DC/DC Switch Mode Power Supply (SMPS) energy is lost every time the power transistor is turned on and off. The switching loss thus increases with switching frequency. This problem has led to the combination of power electronics and radio frequency technology, known as resonant power converters. The advantages are the elimination of switching losses, using Zero Voltage Switching (ZVS) and in some cases also Zero Current Switching (ZCS). The technology has proved itself, with switching frequencies in the Very High Frequency (VHF) band [1]–[4]. So far this has mainly been applied to LED drivers [5]–[7], but has far more possible applications. The energy storing components are small enough that integration onto a silicon wafer is possible. Achieving a fully integrated SMPS would be useful in e.g. cellphone applications, where size and high production volume are important parameters.

In [8] two types of integrated power supplies are defined, Power Supply in Package (PwrSiP) and Power Supply on Chip (PwrSoC). PwrSiP integrates the power transistors and control circuitry monolithically, with the energy storage integrated into the package, e.g. [9]. There are various products available on the market, from several companies, [10]–[14] that implement power supplies in complete packaging. PwrSoC has all the components integrated into the same die. The advantage of the fully monolithic converter is reduced parasitic capacitance and inductance generated from connections needed in the PwrSiP solution. This is important when increasing the switching frequency above 100 MHz [1]. On the other hand the quality of most inductors on chips today are very low. A possible solution would be excluding the inductors using a switched capacitor network [15], [16], however these are often not efficient outside their optimum voltage conversion ratio [17]. Achieving an efficient PwrSoC solution would require an inductor having a high quality factor [8], [18]. The PwrSiP products available have power densities of 0.2-0.5 W/mm^3, and efficiencies around 90-95 % [8]. PwrSoC is still a very new concept, and research have achieved power densities comparable to the PwrSiP products with efficiencies ranging from 30-80 % [8]. Dibene et.al. [19] presents a 400 A PwrSoC with a power density of 8 W/mm^3, and an efficiency just below 80 %, using multiple phases, and advanced control mechanisms.

A possible application within the field of cellphones is a power supply for an audio amplifier. There are many ways to amplify audio from an inherently inefficient class AB amplifier to the ideally lossless class D amplifier [20]. The quiescent current in the class AB topology generates constant losses, making it undesirable for a cellphone application. The more commonly used class D amplifier is, due to the Pulsed-Width Modulation (PWM) technique, ideally lossless. However a side effect of the PWM is increased EMI [21]. If a power supply is designed to only deliver the required power of a class AB amplifier, eliminating the quiescent current, then efficiencies can be increased from the maximum of 78.5 % to ideally 100 %. This is effectively known as a class H amplifier.

This paper presents an integrated class E resonant power converter supplying a class AB audio amplifier. It is supplying a maximum output voltage of 6 V from a Li-Ion battery, assumed to have constant 3.7 V input. The output power is

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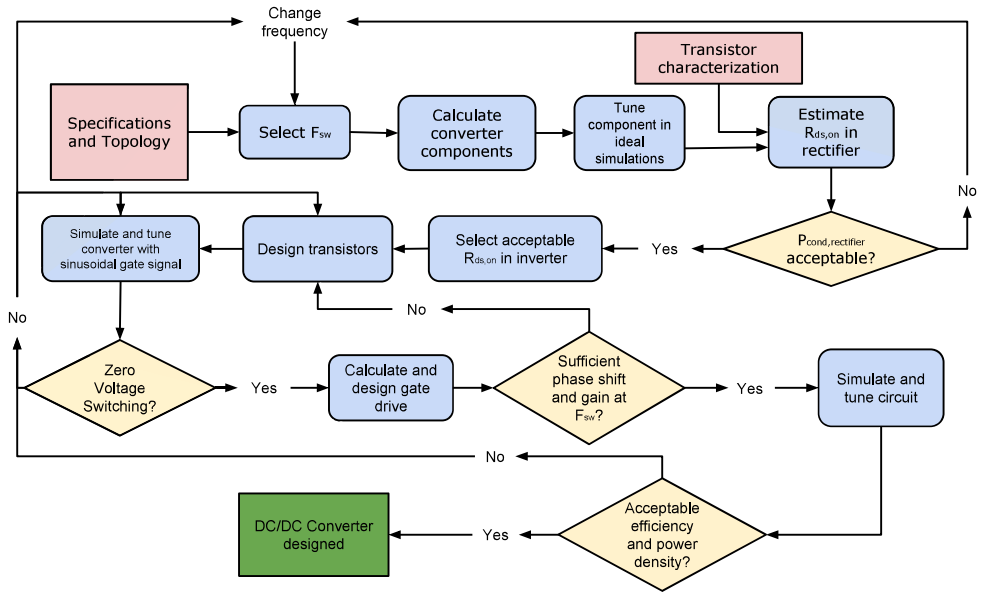


Fig. 1. Flowchart describing the design procedure of an integrated VHF resonant power supply

TABLE I
SPECIFICATIONS FOR THE POWER SUPPLY

V_{in}	3.7 V
V_{out}	6 V
P_{out}	9 W
Process	20 V 0.18 μm CMOS

9 W in a 4 Ω speaker. The power supply is designed in a 20 V 0.18 μm CMOS process, with a listed breakdown voltage of 27 V. The specs can be seen in table I. It is noted that for this to be used in a class H amplifier, it should track an audio sample, and supply the output accordingly. The design of the tracking circuitry has not been carried out.

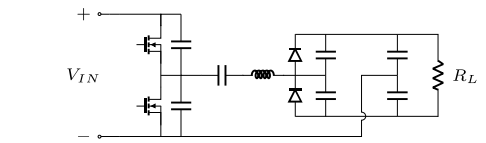
Section II presents the design flow for the resonant power converter. The converter topology will be discussed and presented in section II-A. The power losses are introduced in section II-B. The device parasitics are discussed and a method for extracting them is presented in section II-C. Section II-D presents the self-oscillating gate drive, along with the mathematical equations underpinning its operation. Section II-E discusses inductors on a chip which is followed by section III, where the final design is presented, and the results of the simulations are shown. Finally, section IV concludes on the achieved results.

II. DESIGN PROCEDURE

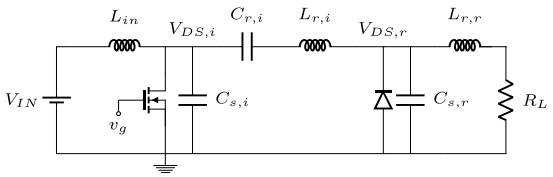
The design procedure is presented in fig. 1. All the relevant theories will be presented in-depth in the following. This procedure was developed for designing a Class E resonant converter. Similar theories applies to other resonant power converters, and the procedure can be modified to fit the relevant equations. The main design variable in this procedure is the frequency. When a switching frequency has been selected the component values are calculated and tuned in ideal simulations. The higher the frequency, the smaller the converter. However in most resonant power converters the output capacitance of a transistor is used as a design parameter [1], [5]. This capacitance is proportional to the size of the transistor, which again is inversely proportional to the drain source resistance of the transistor. At higher frequencies the requirements for smaller capacitances results in higher conduction losses. This will set the first limitation. Following this, the losses in the inverter are calculated, and the transistor in the inverter is designed accordingly. Some tuning of the resonant components might be necessary after introducing the models of the power transistors. When this has been done, the self-oscillating gate drive can be designed. If the gate drive can not achieve a desired phase shift and gain, the designer must redesign the transistors. Final simulations must be carried out, to confirm a working and acceptable power converter. If one is unable to obtain ZVS or an acceptable efficiency and power density, the designer must either redesign the transistors, or ultimately limit the switching frequency of the converter.

A. Converter Topology

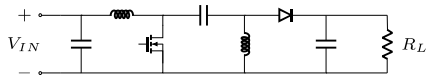
The topology selection is limited to the resonant power converters. Among these, three topologies are often used in the VHF range; the class DE [22]–[24], SEPIC [25]–[27], and class E converter [28], [29], shown in fig. 2. They all work in a similar way with an inverter and a rectifier part. For the class DE and class E the inverter and rectifier can be interchanged. While the class DE converter (fig. 2a) only contains one resonant inductor, preferable in an integrated circuit, it also has three high side semiconductors. High side semiconductors, on a silicon wafer, requires their own wells, which is difficult to implement, and involves more advanced



(a) Class DE converter



(b) Class E converter



(c) SEPIC converter

Fig. 2. Resonant Power Converters

processes, such as triple well or Silicon on Insulator (SOI). Furthermore, it adds parasitic capacitances through body and substrate, which will complicate higher frequency design.

The SEPIC converter (fig. 2c) also has a high side diode. It does have one less inductor compared to the class E, and the trade off between one less inductor and a high side diode could be investigated further. However, diodes capable of working in frequencies above 100 MHz are not commonly available in CMOS design kits. At very high frequencies, the conductivity modulation of power diodes has a tremendous contribution in the total loss. This effect was described in [30], [31]. Schottky diodes are the most suitable devices for very high frequency converters due to their low forward voltage drop and high switching speeds. Even with discrete schottky diodes, which outperform the integrated devices, forward recovery voltage is very severe. For a few nanoseconds the forward voltage increases by 50 %, generating unacceptable losses [32]. In high output voltage, low output current applications, diodes might be favorable.

Consequently the class E converter (fig. 2b) is deemed the most feasible to investigate for an integrating purpose, even though it has three inductors in total. The rectifier is usually implemented with a diode, but it can be exchanged for a synchronous transistor, avoiding the requirements of a diode capable of handling the high frequency. The shunt capacitances $C_{s,i}$ and $C_{s,r}$ of the inverter and the rectifier respectively at higher frequencies are so small that they are realized using the parasitic capacitances of the MOSFETs. In the inverter the input inductor is designed to match the shunt capacitance of the transistor. In the rectifier the transistor is designed such that the output capacitance matches the selected switching frequency.

1) Class E Inverter: The class E inverter has two conditions in relation to the load, R_i, and the shunt capacitance, $C_{s,i}$, that must be met, to achieve both ZVS and ZCS. From [33] they are given in (1) and (2) at the bottom of this page. D_{inv} is the duty cycle of the inverter, f_s is the switching frequency and ϕ_i, the phase of the current, is given by:

$$\phi_i = \pi + \arctan\left(\frac{\cos\left(2\,\pi\,D_{inv}\right) - 1}{2\,\pi\,\left(1 - D_{inv}\right) + \sin\left(2\,\pi\,D_{inv}\right)}\right) \quad (3)$$

In the VHF inverter the shunt capacitance needed to achieve both ZVS and ZCS often is much lower than any achievable output capacitance of the MOSFET. The size of the transistor determines the output capacitance, and the drain-to-source resistance $R_{ds,on}$. Designing for a very low output capacitance requires a small transistor resulting in a higher $R_{ds,on}$. As a result the requirements for the frequency are hard to meet. Adjusting the input inductance can however compensate for this requirement, to ensure that ZVS is still achieved. This is well described in [34]. The load, R_i, on the inverter is simpler to achieve, either by designing the rectifier accordingly, or adding a matching circuit [35]. The latter is not explored in this paper.

The components are calculated from [36]. Assuming that the voltage across the drain-source of the transistor is half a sine wave when it is on, and zero otherwise, the RMS voltage of transistor drain-to-source can be calculated from (4). The output RMS voltage is calculated from the required load and output power (5). The required reactance of the reactance circuit can then be calculated from (6).

$$V_{DS,i,rms} = V_{IN}\,\frac{\pi}{2\,(1 - D_{inv})}\,\sqrt{\frac{(1 - D_{inv})}{2}} \quad (4)$$

$$V_{DS,r,rms} = \sqrt{P_{OUT}\,R_i} \quad (5)$$

$$\begin{aligned} X_{RC} &= R_i\,\sqrt{\left(\frac{V_{DS,i,rms}}{V_{DS,r,rms}}\right)^2 - 1} \\ &= \omega_r\,L_{r,i} - \frac{1}{\omega_r\,C_{r,i}} \end{aligned} \quad (6)$$

The RMS voltage of the output cannot exceed the RMS voltage of the drain-source voltage of the transistor. This gives rises to some limits on the duty cycle when the class E inverter is working in a step-up configuration. The needed inductance

$$R_i = \frac{2\,\sin^2(\pi D_{inv})\,\sin^2(\pi D_{inv} + \phi_i)}{\pi^2\,(1 - D_{inv})^2} \cdot \frac{{V_{IN}}^2}{P_{out}} \quad (1)$$

$$f_{s,max} = \left(\frac{(1 - D_{inv})^2\,\pi}{\tan(\pi D_{inv})\,\tan(\pi D_{inv} + \phi_i)}\,\frac{(1 - D_{inv})}{\tan(\pi D_{inv} + \phi_i)}\right) \cdot \frac{P_{out}}{2\,\pi\,C_{s,i}\,{V_{IN}}^2} \quad (2)$$

and capacitance in the resonant tank is found using the right hand side of (6), ω_r is resonance frequency of the LC tank:

$$\omega_r = \frac{2\,\pi\,f_s}{2\,(1-D_{inv})} \tag{7}$$

To ensure ZVS L_{in} is designed to match reactance of the output capacitance of the transistor and resonance tank [34]. The output capacitance is scaled to its effective capacitance, $C_{s,eff} = {C_{s,i}}/{(1-D_{inv})}$. [5].

$$\frac{1}{\omega_r\,C_{s,eff}} = \frac{1}{\frac{1}{\omega_r\,L_{in}} + \frac{1}{X_{RC}}} \Leftrightarrow$$
$$L_{in} = \frac{1}{\omega_r\left(\omega_r\,C_{s,eff} - \frac{1}{X_{RC}}\right)} \tag{8}$$

The output capacitance is assumed linear, ignoring its voltage dependencies.

2) Class E Rectifier: In the class E rectifier the passive components are designed in such a way that the rectifier is seen as a resistive load at the switching frequency [35]. The current into the rectifier is assumed to be sinusoidal. From [33] the shunt capacitance and resonance inductance, is given in (9) at the bottom of this page. The loading of the inverter is important to achieve ZVS. The components calculated ensure that the input resistance to the rectifier, R_i, is resistive at the desired switching frequency. The required input impedance of the rectifier is achieved by adjusting the duty cycle [2]. See (10) at the bottom of the current page.

3) Components: With the above described equations a set of components can be calculated, and through simulation tune them, to achieve ZVS. To achieve the correct loading the duty cycles of the inverter and rectifier is selected as close to 50 %, which is a requirement for the used gate drive. From (1) and (10) the two duty cycles are connected, to achieve optimum performance. If a duty cycle in the inverter of 60 % is chosen, then the calculated duty cycle in the rectifier is 43 %. The calculated and simulated components is listed in table II. The simulated components had to be tuned. The output power of the calculated inverter was lower than expected, due to not having pure sinusoidal current in the tank, and to increase it the resonance inductance $L_{r,i}$ was increased. To match the effect of the increased inductance, the input choke L_{in}, was adjusted, to ensure ZVS.

TABLE II
CALCULATED AND SIMULATED COMPONENT-VALUES OF A 250 MHZ CLASS E CONVERTER

Inverter		
Component	Calculated	Simulated
L_{in}	455 pH	750 pH
$C_{s,i}$	300 pF	300 pF
$C_{r,i}$	300 pF	300 pF
$L_{r,i}$	2.3 nH	3.5 nH
Rectifier		
Component	Calculated	Simulated
R_i	1.43 Ω	-
$C_{s,r}$	120 pF	140 pF
$L_{r,r}$	4.49 nH	4.5 nH
C_{out}	80 nF	80 nF

B. Power Loss Estimation in MOSFET

The resonant power conversion eliminates the switching losses known from hard switching applications. From [37] the power losses associated with a MOSFET in a resonant power converter can be separated into three parts - the conduction loss, the off-state conduction loss due to the ESR in the shunt capacitance of the MOSFET, and the gate losses determined by the gate resistance and input capacitance.

$$P_{cond} = R_{ds,on}\,{I_{sw,rms}}^2 \tag{11}$$
$$P_{off,cond} = \left(\frac{I_{off,rms}}{C_{OSS}+C_{ext}}\right)^2 R_{OSS}\,{C_{OSS}}^2 \tag{12}$$
$$P_{gate} = 2\,\left(\pi\,V_{gate,AC-pk}\,f_{sw}\right)^2\,R_g\,{C_{ISS}}^2 \tag{13}$$

R_{OSS} is the series resistance associated with the shunt capacitance. The capacitances C_{ISS} and C_{OSS} are the collective capacitance seen on gate and drain respectively.

$$C_{OSS} = C_{gd} + C_{ds}$$
$$C_{ISS} = C_{gd} + C_{gs}$$

The total loss from the transistor is:

$$P_{tot,sw} = P_{cond} + P_{off,cond} + P_{gate} \tag{14}$$

C. Characterization of Transistor

When designing a class E converter with discrete components the choice of transistors are limited to commercially available discrete parts. Often the transistor is described with the needed parameters available from the data sheet. In the integrated circuit the parameters required to design a DC-DC converter are not readily available. Many of the available process technologies have different purposes, and extracting the parameters directly from the documentation are tedious and time consuming. Therefore, another method is necessary.

The voltage stresses on the switches in a class E converter are often four times the input or output voltages [33]. To

$$C_r = \frac{1}{2\pi\,\omega_r\,R_L}\cdot\left(1-2\pi^2(1-D_{rec})^2-\cos\left(2\pi D_{rec}\right)+\frac{[2\pi(1-D_{rec})+\sin\left(2\pi D_{rec}\right)]^2}{1-\cos\left(2\pi D_{rec}\right)}\right) \quad \wedge \quad L_r = \frac{1}{{\omega_r}^2\,C_r} \tag{9}$$

$$\frac{R_i}{R_L} = 2\sin^2(\phi_r) \Leftrightarrow \sqrt{\frac{R_i}{2\,R_L}} = \arctan\left(\frac{1-\cos\left(2\,\pi\,D_{rec}\right)}{2\,\pi\,\left(1-D_{rec}\right)+\sin\left(2\,\pi\,D_{rec}\right)}\right) \tag{10}$$

support this a technology with medium to high voltage capabilities was necessary. In this design a 0.18 μm 20 V process was used, with a breakdown voltage of 27 V. The simulation models available are level 49 HSPICE models, which are an enhanced BSIM3V3 model, especially for use with HSPICE.

The six most important parasitics of the transistor are the gate- (R_g) and drain-source ($R_{ds,on}$) resistance and the gate-source- , gate-drain- and drain-source capacitances (C_{gs}, C_{gd} and C_{ds} respectively). Lastly the series resistance associated with the drain-source capacitance, R_{OSS}, is important to determine the off state losses. Fig. 3 illustrates the most important parasitics.

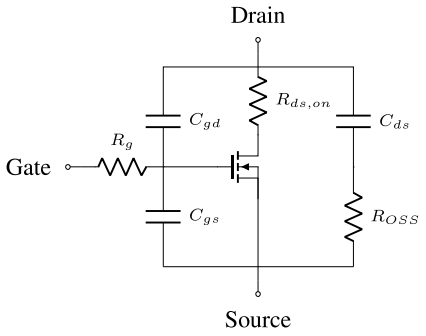


Fig. 3. Transistor with Parasitic Components

To extract the parasitics of the transistor, the two-port Z-parameter analysis is used. It is noted that the Z-parameter method creates a small signal equivalent model; however, by sweeping the frequencies and voltages, the large signal behavior can be derived [37], [38].

The described method of analyzing a circuit is done with a network-analyzer. It is often used in characterization of RF MOSFETs e.g [39]–[43] at frequencies above 10 GHz. These models are much more detailed than those of regular power MOSFETs. In the following, the simplest possible setup and analysis is described and the method is verified with a known device.

The two ports are connected to gate-source and drain-source respectively. Two equations govern the voltages, here shown on matrix-form:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \Leftrightarrow \vec{\mathbf{V}} = \vec{\mathbf{Z}} \cdot \vec{\mathbf{I}} \tag{15}$$

Now applying current vectors, the expression for each Z-parameter in the matrix can be derived. To find the capacitances, the resistive parts of the circuit is ignored - see (16). Similarly the other parameters are derived, and the desired impedances are isolated in (17), (18) and (19).

$$Z_{C_{gs}} = \Im\{-\frac{z_{11}z_{22} - z_{12}z_{21}}{z_{21} - z_{22}}\} \tag{17}$$

$$Z_{C_{gd}} = \Im\{\frac{z_{11}z_{22} - z_{12}z_{21}}{z_{21}}\} \tag{18}$$

$$Z_{C_{ds}} = \Im\{\frac{z_{11}z_{22} - z_{12}z_{21}}{z_{11} - z_{21}}\} \tag{19}$$

Note that in the above equations the parameters z_{mn} are only the imaginary part of the Z-parameters, giving the capacitances. For the resistive elements R_g and R_{OSS}, the S-parameter measures are more complicated. The gate resistance can be estimated from the parameter z_{11}. The z_{22} parameter are at $V_{gs} \geq V_{th}$ equal to the drain source on resitance of the device. At $V_{gs} \leq V_{th}$, and ignoring the restive influence on the capacitances, R_{OSS} can be estimated using (21).

$$\Re\{z_{11}\} = R_g \tag{20}$$

$$\Re\{z_{22}\} = \begin{cases} \dfrac{1}{R_{OSS} \cdot {C_{gd}}^2 \cdot \omega^2} & \text{, for } V_{gs} = 0 \quad (21) \\ R_{ds,on} & \text{, for } V_{gs} > V_{th} \quad (22) \end{cases}$$

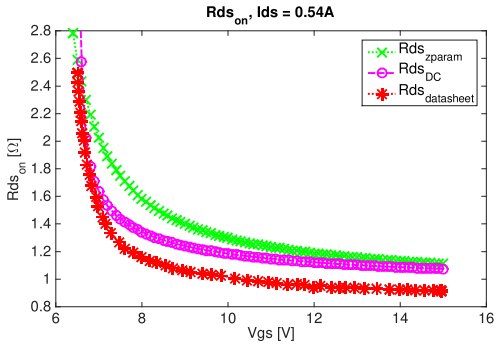
Another method to extract $R_{ds,on}$ is to use a DC current-source connected at the drain, sweeping the gate voltage, and sampling the drain voltage. This gives some limitations to how the models work, because they are forced in saturation. To avoid this, instead a small voltage on the drain will keep the transistor in its linear region, where it is used, and sweeping the gate-voltage, the current is read. This method is used for extracting the parameters of the designed device.

1) Verification of Characterization: To verify that this way of measuring the parasitics is correct, a IRF5802 from International Rectifier with a highly detailed datasheet and SPICE model was used. The datasheet for IRF5802 contains graphs of $R_{ds,on}$ vs. gate-source voltage (V_{gs}), and capacitances C_{iss}, C_{oss} and C_{rss} vs. drain-source voltage (V_{ds}). Its SPICE model is a sub circuit, modeled to the behavior of the device at 1 MHz.

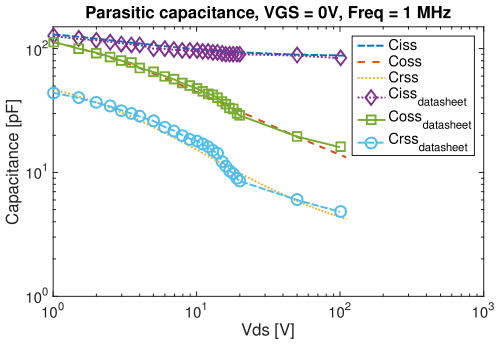
In the datasheet the capacitances are measured at 1 MHz and a gate-source voltage of 0 V, and the simulation and measurements are carried out with the same conditions. Fig. 4 shows the results of the simulations and datasheet values. The capacitances fit their datasheet values. For the $R_{ds,on}$ values the Z-parameter analysis does not accurately produce the same results as the datasheet in values of $V_{gs} < 10$ V; on the other hand, the method described in the datasheet, with a DC current source, produce close to the expected results.

Furthermore, measurements of the IRF5802 was carried out, to confirm the simulations. It was done using a Agilent 4396B network analyzer together with a HP 85046A S-parameter Test set. The measurement circuit can be seen in fig. 5a and the resulting measured capacitances can be seen in fig. 5b. The measured data matches the datasheet values.

$$v_1\Big|_{i_2=0} = \Im\{z_{11}\} \cdot i_1 = Z_{C_{gs}} \cdot i_{C_{gs}} = Z_{C_{gs}} \cdot \frac{Z_{C_{gd}} + Z_{C_{ds}}}{Z_{C_{gd}} + Z_{C_{ds}} + Z_{C_{gs}}} \cdot i_1 \Rightarrow \Im\{z_{11}\} = Z_{C_{gs}} \cdot \frac{Z_{C_{gd}} + Z_{C_{ds}}}{Z_{C_{gd}} + Z_{C_{ds}} + Z_{C_{gs}}} \tag{16}$$

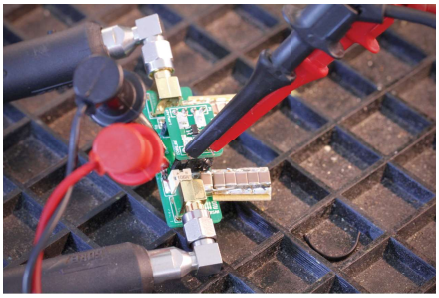


(a) $R_{ds,on}$ *vs.* V_{gs}

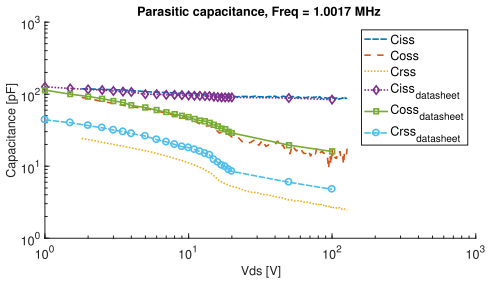


(b) Capacitances vs. V_{ds}

Fig. 4. Simulated results of the Z-parameter analysis



(a) Picture of measurement circuit



(b) Measured Capacitances using the proposed Z-parameter analysis. ($V_{gs} = 0$)

Fig. 5. Measurement of IRF5802

2) Transistor Estimation: To ease the process of estimating the parameters of the transistor, a unit-transistor with an $R_{ds,on}$ of 1 Ω is designed. Parallel coupling two 1-Ω-unit (2x1-Ω-unit) transistors halves the $R_{ds,on}$ and doubles the capacitance. The simulated results is shown in fig. 6 and 7.

Fig. 6 shows the resistances. Both methods of extracting the $R_{ds,on}$ produce similar results. At 5 V gate-to-source voltage the expected on-resistance is approximately 1 Ω.

Fig. 7 provides the capacitances - both versus voltage and frequency. The gate-drain and gate-source capacitance are linear over the voltage. While this is the results of the model, experimental data might reveal some non-linearities. However, as these devices are vertical CMOS devices, their gate-related capacitances are often more linear, than what is known from often lateral power MOSFET. The drain to source capacitance vary largely over both frequency and voltage.

The results of z_{22} parameter at V_{gs} = 0, reveal a large resistance associated with the drain-source capacitance of 3.75 Ω. This resistance will result in off state losses. The resulting parasitic elements of the unit transistor are summarized in table III.

TABLE III
PARASITIC ELEMENTS OF THE 1 Ω $R_{ds,on}$ UNIT TRANSISTOR

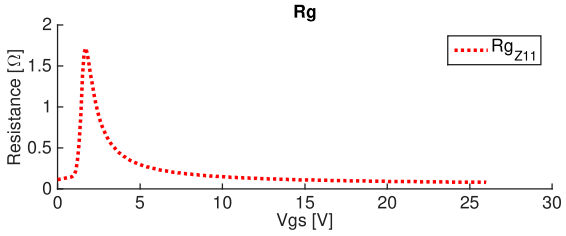
Parasitic element	Value	Unit	Notes
$R_{ds,on}$	1.144	Ω	@ V_{gs} = 5 V
R_g	298	$m\Omega$	
R_{OSS}	3.75	Ω	@ V_{gs} = 0 V
C_{gs}	28	pF	@ V_{ds} = 5 V, Freq = 250 MHz
C_{gd}	6	pF	
C_{ds}	18.48	pF	

D. Driving the Transistor

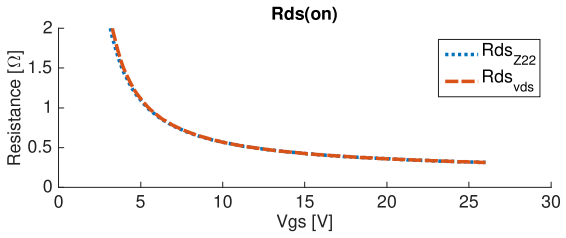
Driving a transistor at high frequency is a challenge. In VHF converters it is very impractical to drive the gate with a PWM signal. There are several methods to drive the gate, either with an externally generated signal, or with a self-oscillating circuit. Externally gate drives are used in implementation such as [29], [44]. One self-oscillating gate drive, commonly used in the class E converter is the class E oscillator, described in [2], [4], [28]. This procedure involves making a feedback circuit, through advanced analytic approach, but limits the duty cycle to 0.5 making it unsuitable for this design.

Recently though a new passive gate drive has been introduced in [5] and used in among others [1], [45]. In design aspects it looks like the class E oscillator, but is simpler. It is effectively an LC-filter generated by utilizing the capacitances of the MOSFET and introducing a gate-inductor. Looking at fig. 3 a schematic of the parasitics can be drawn and introducing a gate inductance, L_g, to achieve the desired filter. Fig. 8a shows the schematic for the described gate drive.

In resonant power converters, the drain voltage of the

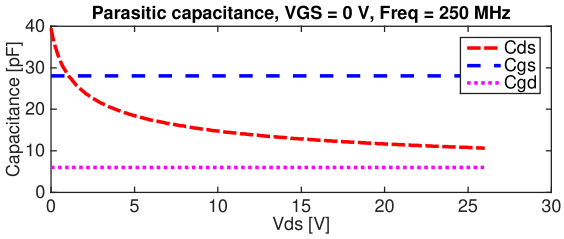


(a) R_g

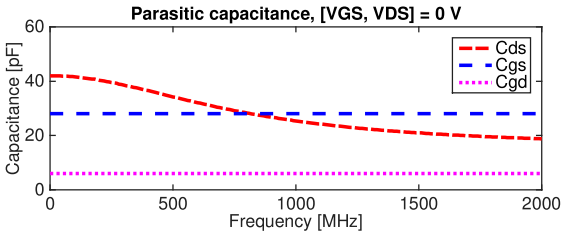


(b) $R_{ds,on}$

Fig. 6. Resistance of the 1-Ω Unit-transistor



(a) Capacitances vs. V_{ds} (Frequency = 250 MHz)



(b) Capacitances vs. Frequency (V_{gs} & $V_{ds} = 0$)

Fig. 7. Capacitances of the 1-Ω Unit-transistor

transistors are close to half a sinusoidal. The added gate inductance creates a filter, with the transfer function from drain to gate shown in (23). Adjusting the inductance the poles of the filter are placed 5-10 % higher than the switching frequency, resulting in a phase shift of the drain signal as close to 180 ° as possible. This will ensure the gate signal turning on, when the voltage on the drain is zero. An added bias voltage can be tuned such that the correct duty cycle is achieved.

$$H_{Lg}(s) = \frac{(L_g\, s + R_g)\, C_{gd}\, s}{L_g\, s^2 + R_g\, s + \frac{1}{C_{gd}+C_{gs}}} \tag{23}$$

The introduced gate inductance will in most cases be able to give the desired phase shift at the chosen frequency. It is clear, that two zeros occur, at s = 0 and s = $-\frac{Rg}{Lg}$. Neither of these zeros contain any imaginary parts, and the resulting frequency at which they occur is both 0.

From (23) the poles of the system is found:

$$s_{pole} = \frac{-R_g \pm \sqrt{{R_g}^2 - \frac{4\,L_g}{C_{gs}+C_{gd}}}}{2\,L_g} \tag{24}$$

The poles are a complex pole pair. To determine the frequency the real and imaginary parts are found, and from the imaginary parts the frequency is found:

$$f_{pole} = \pm\frac{\Im(s_{pole})}{2\,\pi} = \pm\frac{\sqrt{{R_g}^2 - \frac{4\,L_g}{C_{gs}+C_{gd}}}}{4\,\pi\,L_g} \tag{25}$$

If the attenuation achieved at the switching frequency is too high, or low, for a desired gate signal, then external capacitors can be introduced. Fig. 8b and 8c shows the schematics of the gate drives, and the transfer functions are found in (26) and (29). The zeros of these transfer functions are found using (27), (28) and (30), (31) respectively. All these equations are found at the bottom of the current page.

$$H_{Lg+Cl}(s) = \frac{(C_l\, L_g\, R_g\, s^2 + L_g\, s + R_g)\, C_{gd}\, s}{C_l\, L_g\, R_g\, s^3 + (1 + C_l)\, L_g\, s^2 + R_g\, s + \frac{1}{C_{gd}+C_{gs}}} \tag{26}$$

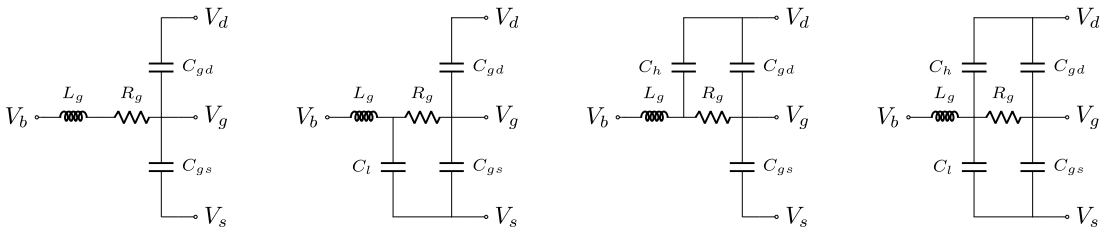
$$z_{1,Lg+Cl} = 0 \tag{27}$$

$$z_{2,Lg+Cl} = -\left(\frac{L_g \pm \sqrt{L_g\,\left(L_g + 4\,C_l\,{R_g}^2\right)}}{2\,C_l\,L_g\,R_g}\right) \tag{28}$$

$$H_{Lg+Ch}(s) = \frac{(C_h\, L_g\, R_g\, s^2 + L_g\, s + R_g)\, C_{gd}\, s + C_h\, L_g\, s^2}{C_h\, L_g\, R_g\, s^3 + (1 + C_h)\, L_g\, s^2 + R_g\, s + \frac{1}{C_{gd}+C_{gs}}} \tag{29}$$

$$z_{1,Lg+Ch} = 0 \tag{30}$$

$$z_{2,Lg+Ch} = -\left(\frac{(C_{gd}+C_h)\,L_g \pm \sqrt{L_g\,\left(L_g\,(C_h+C_{gd})^2 - 4\,C_h\,{C_{gd}}^2\,{R_g}^2\right)}}{2\,C_h\,C_{gd}\,L_g\,R_g}\right) \tag{31}$$



(a) Gate Inductor (b) Ext. Cap. to source (c) Ext. Cap. to drain (d) Both Ext. Cap.

Fig. 8. Passive Gate Drives

For small values of the gate resistance these zeros are all real, so their effect will be minimal at very high frequencies. Even further any zeros effect from a higher gate resistances, can be adjusted by adding the capacitances to the gate-drain of the signal. The poles of the system are solutions to a third order polynomial, and analytically hard to interpret. From [5] a good approximation of the frequency of the pole is:

$$f_p \simeq \frac{1}{2\,\pi\sqrt{L_g\,(C_{ext}+C_{gd}+C_{gs})}} \Leftrightarrow$$
$$L_g \simeq \frac{1}{(2\,\pi\,f_p)^2\,(C_{ext}+C_{gd}+C_{gs})} \tag{32}$$

This is the resonant frequency neglecting the gate resistance. As with the previous gate drives, the resonance frequency is desired to be kept a little higher than the switching frequency of the converter.

The final simple gate drive that can be designed is adding both the external capacitance to source and to drain, shown in fig. 8d. Using external capacitance can be an advantage because it gives the option for more linear capacitances (i.e Metal-Insulator-Metal (MIM) capacitors on chip) than the intrinsic capacitance of the MOSFET, and thus better control of the gate signal. The transfer function of the gate drive with both capacitors is seen in (33).

The zeros are found similarly to the other gate drives, see (34) and (35). The gate resistance has an influence on the zeros, if it is large enough, however this influence can be tuned, by adjusting the external capacitances.

As with the previous gate drives, analytically investigating the poles is unfruitful but using (32) is still a good approximation of the poles frequency. The gate resistance has a very real effect on the achievable phase shift of the gate drive, and in a transistor design should be kept as low as possible to avoid the effects of the zeros.

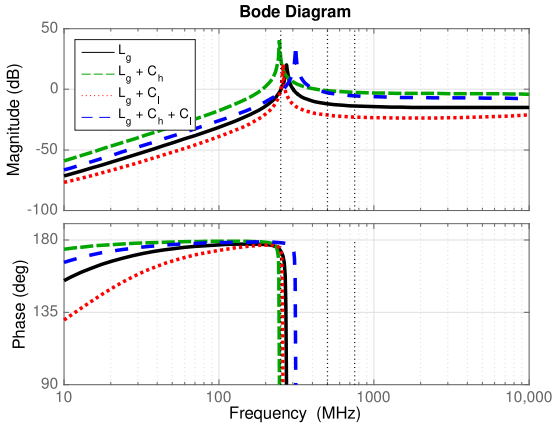


Fig. 9. Gate Drives designed

In table IV the four different gate drives designed are listed. They are all designed for a 10x1-Ω-unit transistor. The design of the gate drives was focused on achieving similar performance, while reducing component sizes. The bode plots of the resulting transfer functions are shown in fig. 9. Adding the external capacitors result in a smaller inductor, a component desired to keep as small as possible, when designing the integrated circuit.

E. Inductors

There is several methods to choose from, when designing an inductor on a chip. From the more simple ones using a planar spiral [46]–[49], to toroids [50], [51], and also using magnetic films to reduce the required size of the inductors [8],

$$H_{Lg+Ch+Cl}(s) = \frac{(C_h+C_l)\,L_g\,R_g\,C_{gd}\,s^3+(C_{gd}+C_h)\,L_g\,s^2+C_{gd}\,R_g\,s}{(C_h+C_l)\,L_g\,R_g\,s^3+(C_h+C_l)\,L_g\,s^2+R_g\,s+\frac{1}{C_{gs}+C_{gd}}} \tag{33}$$

$$z_{1,Lg+Ch+Cl} = 0 \tag{34}$$

$$z_{2,Lg+Ch+Cl} = -\left(\frac{(C_{gd}+C_h)\,L_g \pm \sqrt{L_g\,\left(L_g\,(C_h+C_{gd})^2-4\,(C_h+C_l)\,C_{gd}^2\,R_g^2\right)}}{2\,(C_h+C_l)\,C_{gd}\,L_g\,R_g}\right) \tag{35}$$

TABLE IV
RESULTING COMPONENT SIZES, ATTENUATION AND PHASE SHIFT OF THE GATE DRIVES

	Gate Inductor	Ext. Cap. to source	Ext. Cap to drain	Both Ext. Cap (C_l & C_h)
L_g	1 nH	400 pH	500 pH	250 pH
C_l	-	610 pF	-	300 pF
C_h	-	-	200 pF	400 pF
$\|H\|$ at 250 MHz	-0.77 dB	-0.49 dB	-0.35 dB	-2.03 dB
$\angle H$ at 250 MHz	173.3 $^\circ$	173 $^\circ$	177.5 $^\circ$	178.23 $^\circ$

[18], [19]. The main concern is the achievable Q values - the relation between its inductive value, frequency and resistive value. In an integrated circuit the close proximity to the highly conducting silicon layer results in very high losses from eddy currents induced.

Increase of the Q values is the subject of substantial research. In [49] Q values as high as 50 at 7GHz was achieved. These where, however, constructed in a very fragile structure, and not suitable for most application. Others have tried different shielding methods, to remove the capacitive coupling to the substrate [46]. This limits the self-resonance significantly [52]. The toroidal designs presented in [50], [51] although producing promising results on the Q values of the inductors, as high as 50, the frequencies of these technologies are also currently limited around 10 MHz [8].

The research in this field is in fast development, and is one of the key components to achieving the monolithically integrated power supply. The inductors lack in both modeling for simulations, and in the achievable Q-value. Gardner et. al. [18] made an overview of on-chip inductors, and the only inductors usable in frequencies above 100 MHz are planar spiral structured air inductors. These inductors have not shown Q values above 10. Very recently Ferric Inc. introduced post-processed inductors on chip, capable of handling frequencies at 50-150 MHz, with magnetic thin film [53]. Sturcken et.al. demonstrated in a 1.8V to 1V integrated voltage regulator, with efficiencies $\sim$70 %. [54] These inductors was, however, not available for this work. Lastly, it is worth mentioning that another solution could be bond wires. With inductance values around 1nH/mm and Q values approaching 50 at 1 GHz they are very interesting. Automated setups can keep variations of inductance to within 1% [55]. Nonetheless, in this work, the fully monolithic integration was of highest priority and bond wires were therefore ruled out.

In this paper the lump-model of a spiral inductor on chip is used, obtained from [55], shown in fig. 10. It consist of an inductance L, a series resistance R_s, together with a resistance associated with the eddy-current losses induced in the substrate, R_{eddy}. It has parasitic capacitances both to the substrate, C_{ox} and to the cross under path, C_P, which is needed to connect the innermost winding to the outside. Finally there are parasitics associated with the substrate, both its resistivity, R_1 and capacitance, C_1.

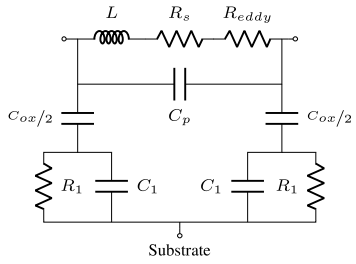


Fig. 10. Inductormodel based on [55]

Three octagonal inductors used in the simulations are here presented. The inductors are all designed from the process parameters for the current process, using the top metal layer, farthest from the silicon, and largest thickness. The results is shown in table V. The Q value of 14 is higher than described in the literature. This is due to the crudeness of the model, and the results would have to be verified before an actual implementation.

Fig. 11 shows the Q value over frequency of the designed inductors. The two larger inductors have an optimum around 200 MHz, and decreases, until their self resonance frequency of approximately 2 GHz at which Q is zero. The 750pH inductor can be seen to have a maximum much higher, at a frequency close to 3 GHz. For all of the above described inductors their self resonance frequency is well above the desired switching frequency of the circuit.

TABLE V
DESIGN OF THE INITIAL INDUCTORS

Inductor	L [H]	R_s $[m\Omega]$	R_{eddy} $[\mu\Omega]$	C_p $[fF]$	C_{ox} $[fF]$	R_1 [Ω]	C_1 $[fF]$	Q @ 250 MHz
L_{in}	750p	193.5	12.4	116.6	303.8	469.5	21.3	6.1
$L_{r,i}$	3.5n	294.8	846.7	859.9	2730	52.14	191.8	15.6
$L_{r,r}$	4.5n	338.7	2010	1070	3920	36.34	275.8	14.8

TABLE VI
DESIGN OF THE FINAL INDUCTORS

Inductor	L [H]	R_s $[m\Omega]$	R_{eddy} $[\mu\Omega]$	C_p $[fF]$	C_{ox} $[fF]$	R_1 [Ω]	C_1 $[fF]$	Q @ 250 MHz	Tr. W. $[\mu m]$	Est. Area $[mm^2]$
L_{in}	550p	200.52	4.26	59.51	159.03	896.83	11.15	4.31	25	0.033
$L_{r,i}$	1.8n	430.19	85.39	107.12	494.75	288.27	34.69	6.52	30	0.15
$L_{r,r}$	4n	581.14	258.09	204.11	912.30	156.33	63.96	10.33	35	0.18
L_{gate}	300p	121.86	2.16	64.27	140.15	1020	9.83	3.87	30	0.031

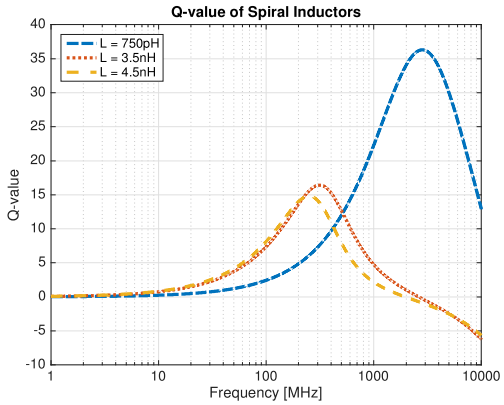


Fig. 11. Q value of the designed Inductors over Frequency

III. Results

Referring back to the design flowchart in fig. 1, a switching frequency has to be selected. To achieve the smallest possible converter, the highest possible switching frequency is desired. From (9) the shunt capacitance in the rectifier is inverse proportional to the frequency. If a switching frequency of 500 MHz is chosen, the resulting capacitance of the transistor will be so small that the resulting drain-source resistance gives a conduction loss above 20 % of the total power.

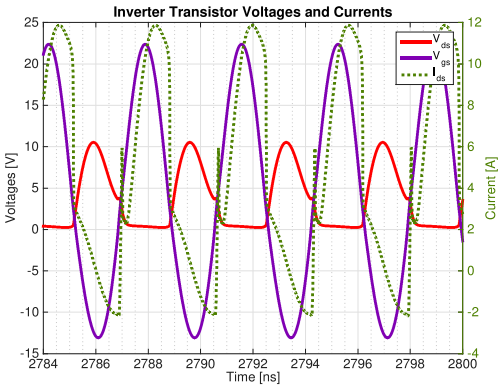
To address this issue, the switching frequency is decreased. Several steps were taken in this design procedure, and three different converters were designed. All designs were made with MIM-capacitors, and ideal inductors.

- A 250 MHz design with 22 parallel coupled 1-Ω-unit transistor in the inverter
- A 150 MHz design with 22 parallel coupled 1-Ω-unit transistor in the inverter
- A 250 MHz design with 10 parallel coupled 1-Ω-unit transistor in the inverter

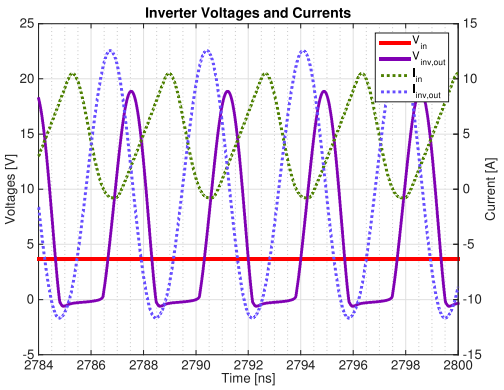
The first design had issues with currents induced through the gate-drain capacitor to the drain channel because of the large capacitive value and a high dv/dt of the gate-signal. As a result two other designs were made, lowering the frequency, and with a smaller device (i.e. lowering the gate capacitance). Although the 150 MHz design showed improvement in terms of efficiency, their respective inductors was twice as large in physical size. The power density became much lower than desired. In the end, the 250 MHz design with the 10x1-Ω-unit transistor was chosen for further implementation, with the self oscillating gate drive because of its smaller size. The results of the converters designed are shown in table VII.

A. 250 MHz Converter with Self Oscillating Gate Drive

The 250 MHz design is implemented with the self-oscillating gate drive with both external capacitors to ground and drain respectively. Fig. 12 and 13 presents the simulation results. The switching frequency achieved is 272 MHz.



(a) Transistor Voltage and Currents



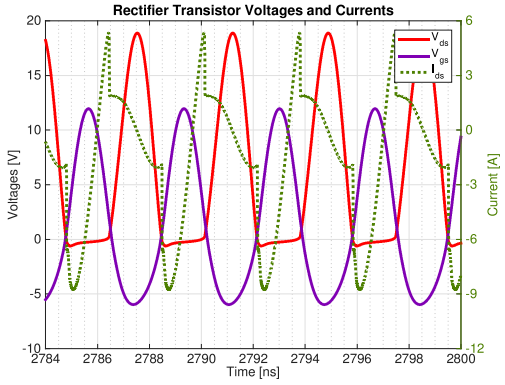
(b) Input and Output Voltage and Currents

Fig. 12. Inverter waveforms of the 250 MHz Converter with Self Oscillating Gate Drive

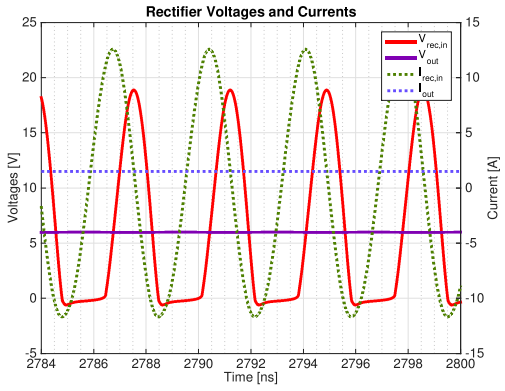
The circuit has been tuned for optimum performance, and the self resonance of the circuit became a little higher. Due to the nature of the self oscillating gate drive, no adjustment is needed in the gate drive. The gate signal has a peak-to-peak

TABLE VII
Summary of Designed Converters

	Inverter			Rectifier			Power	
	$V_{DS,i,pk}$ [V]	$I_{sw,rms}$ [A]	$I_{out,pp}$ [A]	$V_{DS,r,pk}$ [V]	$I_{sw,rms}$ [A]	$I_{out,ripple}$ [mA]	$P_{avg,in}$ [W]	η [%]
250 MHz (22x1Ω-unit transistor)	15.45	8.8	8.52	27.44	2.62	1.22	22.14	43.21
150 MHz (22x1Ω-unit transistor)	14.47	5.32	6.73	27	2.54	3.1	14.71	64.84
250 MHz (10x1Ω-unit transistor)	13.46	6.25	10.56	20.89	2.9	3.62	17.24	52.1



(a) Voltage and Currents



(b) Input and Output Voltage and Currents

Fig. 13. Rectifier waveforms of the 250 MHz Converter with Self Oscillating Gate Drive

amplitude of 33V, and from (13) this will result in a high loss in charging and discharging of the gate capacitances.

The duty cycle achieved is 46 % and 43 % in the inverter and rectifier respectively. The results are close to the expected in the rectifier, but the duty cycle achieved in the inverter is smaller. Tuning the bias to increase the duty cycle unfortunately was not possible, without compromising the breakdown voltage on the gate. The drain current of the transistor is seen to spike just at turn off, and not achieving ZCS. However, ZVS is achieved, naturally by the self-oscillating gate drive. The efficiency of the converter is 55.5 %, which is comparable to other PwrSoC designs [8]. To understand the power losses in the circuit, the losses in the transistors were calculated according to section II-B. The results are presented in table VIII and fig. 14. The RMS currents were extracted from the resulting simulations.

TABLE VIII
POWER LOSSES IN THE TRANSISTORS

	Inverter [W]	Rectifier [W]
P_{cond}	2.15	0.76
$P_{off,cond}$	0.42	0.35
P_{gate}	2.52	0.66
P_{tot}	5.09	1.77

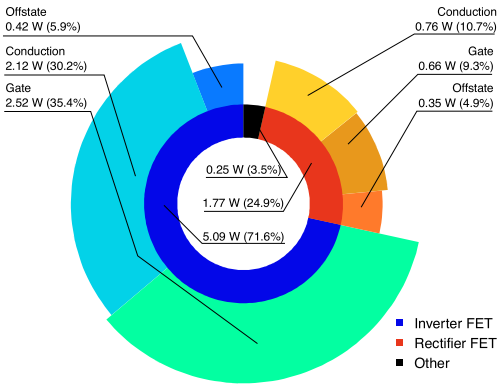


Fig. 14. Power Loss Breakdown in the 250 MHz Converter with Self Oscillating Gate Drive

The total loss in the transistors is close to 6.85 W. The converter has been tuned for an output power of 9 W, and had a total average input power of 16.11 W. The remaining losses of 0.25 W can be contributed to the ESR of the MIM capacitors. The results of the converter with the self oscillating gate drive are shown in table IX.

With a loss of approximately 7W, the design of the thermal handling also becomes important. If 100 K temperature rise is allowed, from ambient, then the thermal resistivity from silicon to the ambient surroundings cannot exceed 14 K/W. The estimated overall size of the final converter, assuming MIM-capacitors of 3 fF/μm^2, and no overlaying of capacitors or inductors, is 28.6 mm^2. This gives a power density of 0.314 W/mm^2.

TABLE IX
SUMMARY OF 250 MHZ CONVERTER WITH 10X1Ω-UNIT TRANSISTOR IN THE INVERTER AND SELF OSCILLATING GATE DRIVE

	Inverter
$V_{ds,pk}$	10.53
$I_{sw,rms}$	7
$I_{out,pp}$	24.25
	Rectifier
$V_{ds,pk}$	18.88
$I_{sw,rms}$	4.13
$I_{out,ripple}$	5.1
	Power
$P_{avg,in}$ [W]	16.11
η [%]	55.54

B. Implementing Inductor Models

The results shown so far have been simulations with ideal inductances. A simulation with the presented model for inductors was carried out. However the inductors are damping the voltages of the circuit, and oscillations were not possible. Fig. 15 presents an AC analysis of the gate drive with the implemented inductors. The added parasitic resistance and capacitance of the inductors effects the gate drive, and a phase shift of over 155° is unachievable. These inductors were designed to the best performance possible, in the available IC

process, and it is very clear that these performances are just not good enough. The best available inductors integrated on chip are currently not much better than that of a standard spiral inductor, so as of right now, a different solution to the inductors has to be found. Increasing the Q factor to 10-20, showed oscillating circuits, however still with poor efficiency. One such solution could be the VHF magnetic inductors, recently introduced by Ferric Inc. [53]. These are limited at 150 MHz, so a reduction of switching frequency is an undesired side-effect. Finally, redistribution layer techniques could be implemented. Inductor values of 80 nH, with Q factors greater than 35 at 100 MHz were reported in [56].

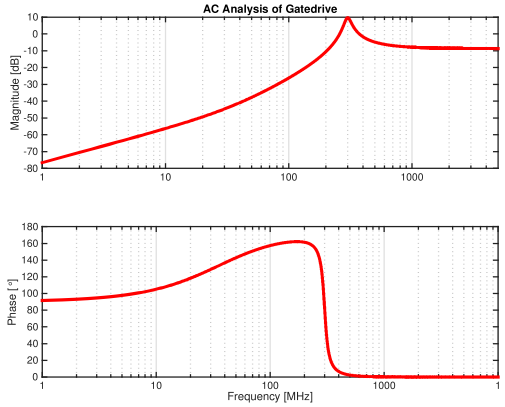


Fig. 15. AC Analysis of the Gate Drive with the Modeled Inductors

IV. Conclusion

To achieve higher power densities switching frequencies have increased. This paper presents an integrated VHF resonant power converter, switching at 250 MHz. The class E topology was deemed the most interesting for integration purposes due to lack of high side power semiconductors. However, limitations in the class E rectifier design and the process selected meant that higher switching frequencies were not desirable because of power losses. From the relations between the frequency, the capacitances in the transistors and their relation to the achievable $R_{ds,on}$, and the power losses in the transistors an optimum frequency for a given load and power can be found. Such an optimum could also find the best achievable inductors, either through the crude models, or using more advanced modeling. This is left for future work.

The two-port Z-parameter method was used to characterize the transistor models, utilizing the internal capacitances of the transistor in the class E converter. Furthermore the design was implemented with the self oscillating gate drive, implemented with external LC-filters. This gate drive was thoroughly mathematically analyzed, revealing the necessity to keep gate resistance at a minimum, to achieve the best performance. The four designed converters were designed for a 9W output power in a 4-Ω load, and efficiencies in the range from 43-64 % were reached. With the self oscillating gate drive the simulated efficiency with ideal inductors was 55 %. The power density based on simulations with ideal inductor models was 0.314 W/mm^2. However implementing models of integrated spiral inductors showed that the added parasitics lowers the performance of the gate drive, eliminating the possibility for ZVS. Other methods of implementing the inductors are necessary, for a working integrated resonant power converter with this type of gate drive.

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Appendix A-J3

Yasser Nour, Hoà Thanh Le, Anpan Han, Flemming Jensen, Ziwei Ouyang, and Arnold Knott, "Microfabricated Air-core Toroidal Inductor in Very High Frequency Power Converters", IEEE Journal of Emerging and Selected Topics in Power Electronics, 2018.

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Microfabricated Air-core Toroidal Inductor In Very High Frequency Power Converters

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***Abstract*— Miniaturization of power supplies is required for future intelligent electronic systems e.g. internet of things devices. Inductors play an essential role, and they are by far the most bulky and expensive components in power supplies. This paper presents a miniaturized microelectromechanical systems (MEMS) inductor and its performance in a very high frequency (VHF) power converter. The MEMS inductor is a silicon-embedded air-core toroidal inductor, and it is constructed with through-silicon vias, suspended copper windings, silicon fixtures, and a silicon support die. The air-core inductors outperform the silicon-core inductors with higher quality factor at higher frequency. This is verified by small-signal measurements. A 20-turn air-core inductor achieved an inductance of 44.6 nH and a quality factor of 13.3 at 33 MHz, while a silicon-core inductor with the same geometry has a quality factor of 9 at 20 MHz. A DC-DC class-E boost converter is designed and implemented using the fabricated MEMS air-core inductor and a high-performance 65 V gallium nitride field effect transistor. The VHF converter achieved a peak efficiency of 78 % at the input voltage of 6.5 V_{DC}. The MEMS inductor can carry 1 A RMS AC current at 33 MHz and delivers 10.5 W to the output.**

***Index Terms*— Microelectromechanical systems, inductor, DC-DC power converters, zero voltage switching, gallium nitride.**

I. Introduction

POWER supplies are essential sub-systems for modern intelligent electronic devices and systems. They are found in customer electronics, light emitting diode (LED) lightings, and internet of things (IoTs) [1]–[3]. Size, weight, life time, and cost are critical for such applications. While most electronic systems have been advanced rapidly with a dramatic decrease in size and cost, power supply technology is lagging behind. Power supplies are still bulky, inefficient, and costly [4]–[6]. Power supply in package (PwrSiP) [5], [6] and power supply on chip (PwrSoC) [5]–[10] are the vision of power supplies with high efficiency, high power density, and low cost.

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Developing integrated power converter requires miniaturization of energy-storing elements and makes them compatible with the processing flow of integrated circuits. Increasing the switching frequency to the very high frequency range (VHF) (30 MHz – 300 MHz) allows the inductance values needed for PwrSoC to drop to tens of nanohenries (nH).

Taking advantages of microelectromechanical systems (MEMS) fabrication technologies, miniaturized silicon-based inductors can be fabricated with high quality factor, high operating frequency, and high inductance thus enabling their usage in power supplies as energy storage elements. There are two categories of microfabricated inductors: magnetic-core and non-magnetic core inductors. Magnetic-core inductors are typically fabricated with magnetic thin films and two-dimensional (2D) windings such as spiral inductor [11], [12] and race track inductor [13]–[16]). Three-dimensional (3D) windings such as solenoid inductor [17], [18], and toroidal inductor [19], [20] are also possible. High inductance density can be achieved with high permeability core materials, but excessive core loss at VHF operating range is still a major challenge.

Air-core inductors are another solution for VHF power supplies. They have the advantage of no core loss and high frequency operation [21]. Previous works reported on air-core inductors including 2D planar inductors [22], [23], on-substrate 3D inductors [24], [25], and substrate-embedded 3D inductors [26], [27]. In many air-core inductors, the silicon substrate fully or partially remained, which causes undesired parasitic capacitance and eddy-current losses. Thus, quality factor and operating frequency are reduced [27]. Therefore, in the ideal air–core inductor design, the entire core must be removed.

Indeed, with the inductance of tens of nH [22], [26], [27], air-core inductors are suitable for VHF converters. Resonant converters allow the utilization of soft switching techniques due to the intrinsic alternating behavior of current, voltage or both by controlling the switches. Soft switching is desired to minimize the switching losses in the semiconductor devices [28]. High-performance gallium nitride field effect transistors (GaN FETs) have shown a great potential for high-voltage, VHF power supplies. GaN FETs have superior gate charge characteristics compared to other semiconductor transistors [29], [30]. The gate charge (Q_G) multiplied by the on-resistance (R_{DS_ON}) figure of merit shows that GaN FETs can be driven easily compared to their silicon counterparts.

A DC-DC resonant converter consists of two stages which include an inverter stage and a rectifier stage. An inverter stage converts the DC input voltage to AC voltage or current, where after a rectifier stage converts AC current or voltage output of the inverter to a DC voltage or current. A common example of a rectifier stage is a class-D current-driven rectifier that was thoroughly studied and presented in [31], [32].

Inverter design is more challenging. Two examples of inverter topologies are class-E and class-D. The advantage of class-E inverter is that only one low side switch is needed to realize a power stage. However, they have a high voltage stress factor across the switch (drain-to-source voltage divided by the input voltage). This voltage stress can be 3.5 to 4 times higher than input supply voltage [33]–[37]. As a result, a high voltage switch with high breakdown voltage is required.

Class-D inverters on the contrary utilize two switches and have lower voltage stress on switches. The voltage stress equals to the input voltage which allows the usage of higher speed, lower voltage devices [36], [38]. To control two switches, precise design of the gate driver circuitry is needed to avoid cross conduction through the switches which may cause catastrophic failure. Other inverter topologies involve extra circuit components to solve the problem of high voltage stress on the switches [34], [36].

In this paper, a new silicon-embedded air-core toroidal inductor is presented. It has minimal parasitic capacitance and no substrate eddy-current losses due to a complete removal of silicon core. The miniaturized inductor is fabricated by an advanced 3D MEMS fabrication process, characterized by small-signal measurement, and demonstrated in a resonant power converter. The resonant boost converter is based on an agile Schottky-diode based class-D current-driven rectifier and a class-E inverter. The MEMS inductor is used in the resonant network, and a 65 V GaN FET is used as a switch. The converter is optimized to operate in zero voltage switching (ZVS) mode for minimal switching losses. Large signal high-frequency performance of the fabricated inductor is tested in terms of electrical and thermal performance, and AC current capability.

The paper is organized as follows. Section II presents the design and fabrication of the silicon-embedded air-core toroidal MEMS inductor. Section III describes small signal characterization of the MEMS inductor. IV presents design and simulation of a class-E boost converter. Converter performance is presented in Section V, and conclusions follow in Section VI.

II. Inductor Design and Fabrication

A. Inductor Design

The proposed design of a MEMS air-core toroidal inductor is shown in Fig. 1. It is constructed with copper-filled through silicon vias (TSVs), suspended top and bottom windings, five silicon fixtures, and a silicon support die. The TSVs are positioned accordingly to toroidal shape with one TSV at the inner ring and two parallel TSVs at the outer ring. The number of fixtures is selected for mechanical stability of the suspended

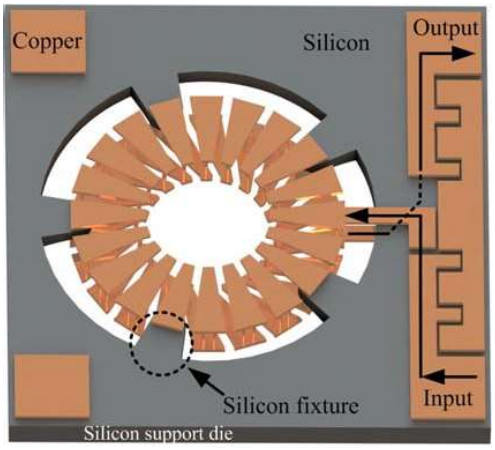


Fig. 1. 3D design of the MEMS air-core toroidal inductor with important features: copper-filled through-silicon vias (TSVs), suspending windings, silicon fixtures, silicon support die, pads for measurement and packaging, and ground-signal-ground probes for wafer-level characterization. The direction of inductor current is depicted by the arrows.

windings. The copper windings are attached to the silicon support die by silicon fixtures that cover outer TSVs and secure the suspended windings. The layout of input and output terminals includes ground-signal-ground pads for on-wafer measurement and two 800 µm x 800 µm pads for connecting to PCB by wire bonding or flip-chip bonding. The direction of current flow is illustrated by the arrows in Fig. 1. The current flows from the input terminal through the windings, comes back to wafer backside, and gets out to the output terminal via through-silicon interconnects as shown by the arrows in Fig. 1.

This air-core design has four main advantages: low parasitic for high Q at high frequency, no substrate eddy-current losses due to a complete removal of silicon core, low electromagnetic interference (EMI) by using self-contained magnetic flux within the toroidal structure, and high compactness with the silicon-embedded construction.

B. Fabrication Technology

The MEMS inductor is fabricated by a novel 3D fabrication process. The process is developed based on MEMS fabrication technologies with the focus on complementary metal oxide semiconductor (CMOS) compatibility, scalability, and flexibility. The inductors can be fabricated with a wide range of geometry and sizes. The process consists of 12 steps and 4 photomasks. The details of fabrication process can be found in our fabrication paper [39]. In this paper, the fabrication process is summarized in four steps (Fig. 2a) as follows.

First, the TSVs are created by deep reactive ion etching (DRIE) (Fig. 2a). A 350-µm-thick silicon wafer is etched through with holes (50 µm diameter) and narrow fixture trenches (3 µm and 7 µm width) which are defined by photolithography. The holes are etched through, while the trenches are not. By the end of step 1, hollow silicon TSVs are created. Second, copper is deposited as the conductive material (Fig. 2b). After depositing insulation layers including aluminum oxide (Al_2O_3) and silicon dioxide (SiO_2), copper is electroplated into the TSVs and on both wafer sides. The

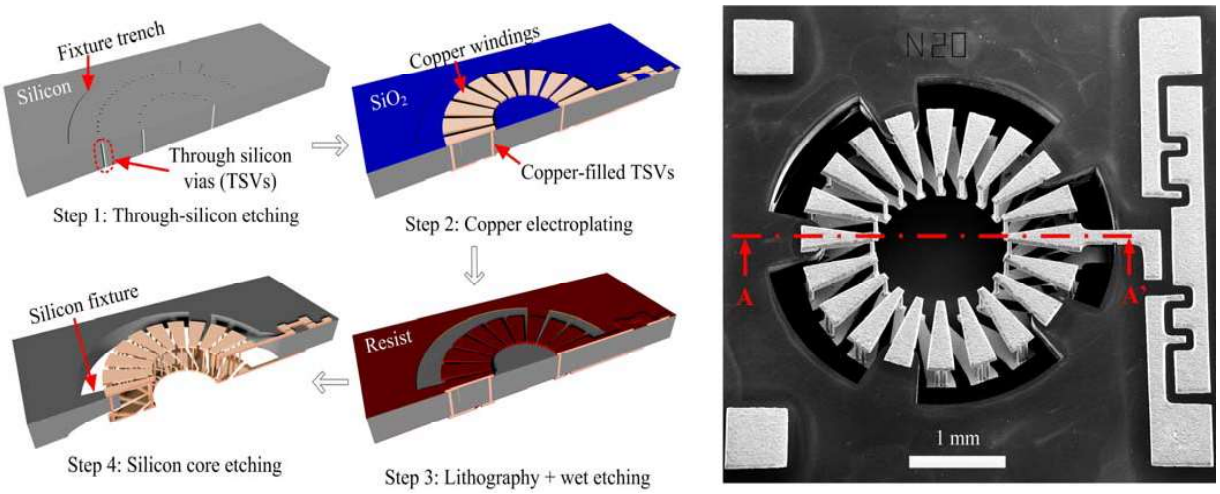


Fig. 2. (a) A four-step fabrication process of MEMS air-core toroidal inductor viewed from direction A-A'. Step 1 is to create 50-µm-diameter through-silicon vias (TSVs) in a 350-µm-thick wafer by deep reactive ion etching and atomic layer deposition. Step 2 includes deposition of insulation layers 50 nm aluminum oxide (Al2O3) and 1.5 µm silicon dioxide (SiO2), electroplating of copper in TSVs and top and bottom conductors, and copper wet etching to define the toroidal windings. Step 3 starts with protecting copper windings by aluminum oxide followed by photolithography of spray-coated resist and wet etching using hydrofluoric acid. Step 4 is to etch the silicon core using dry ICP etching and release the suspended windings by wet etching and drying steps. (b) A secondary electron microscopy (SEM) micrograph of MEMS air-core inductor with 1.5 mm outer diameter, 0.75 mm inner diameter, 20 turns, 350 µm height, and 50 µm TSV diameter. The thickness of top and bottom windings is 50 µm. Winding gap is 94 µm.

aluminum oxide (Al_2O_3) is deposited by atomic layer deposition (ALD) using a process developed for depositing Al_2O_3 on high-aspect-ratio structures [40]. Third, an etching mask is created prior to removal of the silicon core. A 50 nm layer of ALD Al_2O_3 is deposited. Photoresist (AZ 4562, Microchem., USA) is then spray-coated followed by photolithography. It is crucial for the resist to fill and seal the fixture trenches prior to the next Al_2O_3 wet etching step using buffered hydrofluoric acid (BHF). Last, the silicon core is removed using isotropic dry etching by an inductively coupled plasma (ICP) silicon etching tool followed by releasing steps including BHF wet etching, deionized water rinsing, and nitrogen drying. By utilizing Al_2O_3 deposited on the fixture trenches as an etch stop, the silicon core can be removed completely without damaging silicon fixtures. The fixture trenches define the silicon fixtures and support die, thus defining the toroidal core. The process temperature is kept below 200 °C, and this enables post MEMS processing on CMOS wafers and avoid damaging the existing active electronics.

The fabricated MEMS air-core toroidal inductor is shown in Fig. 2. It has 20 turns, 350-µm-tall, and the footprint is 9 mm^2. The silicon core was removed completely while the silicon fixtures and support die remained undamaged. No winding deformation was observed after the releasing steps.

The fabrication process has the advantages of fabricating inductors with a wide range of sizes and shapes. A process yield of 95% was achieved. Magnetic composite core inductors can also be made using the fabricated TSV air-core inductors and a simple screen-printing process. One limitation of the process is a large winding gap of 94 µm due to the Cu wet-etching step. This can be improved by a minor modification in step 2 of the process. For example photoresist is used as a mold for electroplating of Cu.

The thermal and mechanical stability of the fabricated inductors were tested with a thermal cycling test (250 cycles, -45 to 155 °C) and a drop test up to 2 m, respectively. The results are also presented in our fabrication paper [39]. The inductors with the turn/fixture ratio from 6 (30 turns:5 fixtures) to 10 (30 turns:3 fixtures) were tested. They showed good stability after the tests. The suspended windings did not deform and the inductors were still functional. If a higher robustness is required, the air core inductor can be filled with epoxy for stability enhancement.

III. Small Signal Characterization of Inductor

Air-core and silicon-core MEMS inductors were electrically characterized from 0.9 to 110 MHz using a precision impedance analyzer (Agilent 4294A). A dedicated PCB (Fig. 3a) is used as the interface to test the MEMS inductors. An inductor is mounted on the test board using epoxy which is cured at 220 °C for 30 minutes using a convection oven. The inductor input and output terminals are connected to the test board through three 30-µm-diameter gold wires. Impedance analyzer calibration is done with short connection, open connection, and 50 Ω. The calibration boards are shown in Fig. 3b. Short connection is made by three parallel gold wires. Inductance (L), quality factor (Q), and AC resistance (R_{AC}) are measured (Fig. 3c, d).

The air-core inductor has an inductance of 44.6 nH, Q_{peak} of 13.3 at 33.2 MHz. The silicon-core (ρ = 1 - 20 Ωcm) inductor has an inductance of 43.7 nH and lower Q_{peak} of 9 at lower frequency of 20 MHz. The optimal operating frequency of the air-core inductor to be used in the converter is at 33 MHz. At 33 MHz, the AC resistance (R_{AC}) of the air-core inductor is 0.65 Ω which is two times lower compared to 1.25 Ω of the

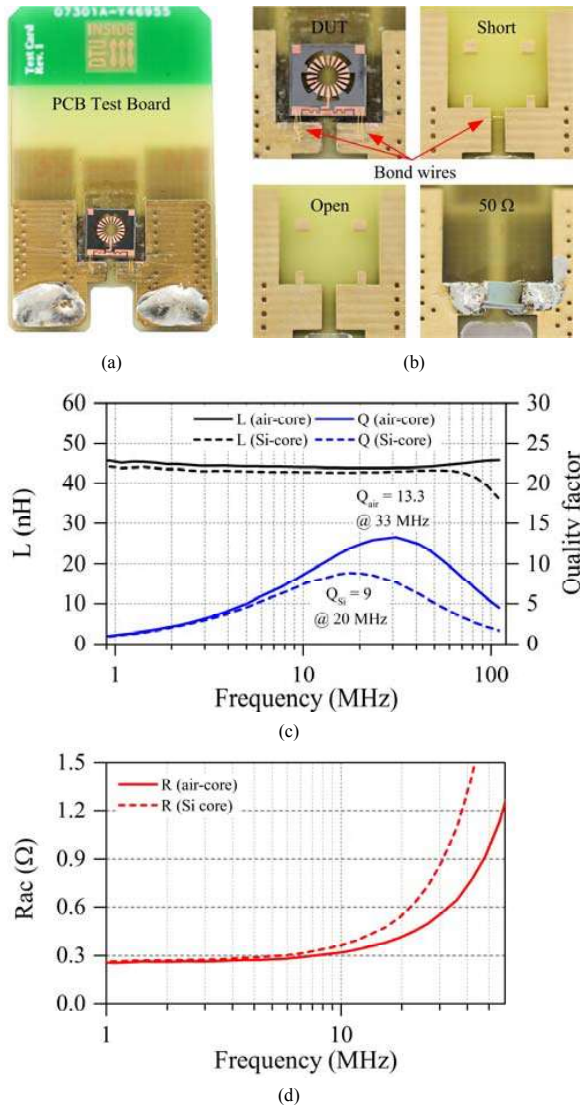


Fig. 3. Small signal characterization of air-core and silicon-core toroidal inductors. (a) PCB test board. An air-core inductor is glue-mounted and connected to the test board through three parallel gold wires. (b) A device under test (DUT) and calibration structures including short connection, open connection, and 50 Ω. (c) Measured inductance (L) and quality factor (Q) in the frequency range from 0.9 MHz to 110 MHz. (d) Measured AC resistance (R_{AC}) in the frequency range from 0.9 MHz to 50 MHz. Air-core and silicon-core inductors have inductance of 44.6 nH and 43.7 nH. Air-core inductor is better than silicon-core inductor with higher Q_{peak} of 13.3 at higher frequency of 33 MHz.

silicon-core inductor. The increase in resistance results in a lower Q factor in the Si-core inductors. This is due to a higher parasitic capacitance and the substrate eddy-current loss of the Si-core inductor. The measured results showed a three-fold higher parasitic capacitance in the Si-core inductor with 11.5 pF compared to 3.7 pF of the air-core inductor, thus allowing the air-core inductor to operate at higher frequency with higher Q factor. This paper focuses on the characterization and demonstration of the fabricated air-core inductors, and the

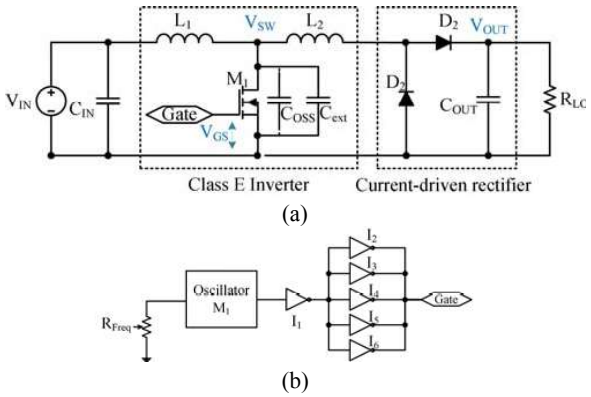


Fig. 4. Circuit diagram of (a) Class E resonant boost converter includes a Class E inverter and a Schottky-diode based class D current driven rectifier. The converter is optimized for zero voltage switching at 33 MHz. (b) frequency-tunable gate driver using silicon oscillator and variable resistor with fixed 50% duty cycle.

models of the air-core toroidal inductors can be found in [41]–[43].

IV. Class-E Resonant Boost Converter

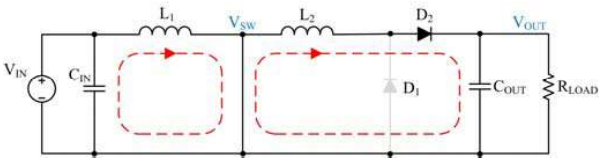
A. Converter Design

To test the inductor, a class-E resonant boost converter has been selected. The converter is designed to operate in ZVS mode at 33 MHz where the inductor has a maximum Q of 13.3, R_{AC} of 0.65 Ω, and L of 44.6 nH. Fig. 4a shows the topology of the resonant converter. The converter consists of two parts: rectifier and inverter.

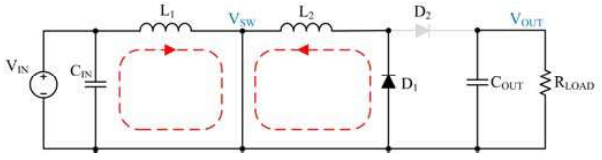
The first part is a class-D current driven rectifier [31], [32] which is used to drive the load resistance. The rectifier allows DC power flow through D_2 to the load and AC power flow through rectification act. A similar concept was reported in [28] where a resonant type rectifier was used instead of class-D in this case. A reported resonant rectifier [28] is not used in this converter to reduce the amplitude of high frequency current flowing in the inductor under test. This will prevent extra AC losses in the inductor. It is beneficial to deal with D_1 as a freewheeling diode when L_2 current becomes negative.

The second part is the inverter which consists of an input choke (L_1), a GaN FET (M_1), a capacitor (C_{ext}) and finally the inductor under test (L_2). The GaN FET is driven by a logic buffer with an output stage of five inverters connected in parallel as shown in Fig. 4b. The frequency is set by a silicon oscillator with a fixed duty cycle of 50 %. L_2 is used as a part of the resonant network, and it also delivers DC current to the load. L_1 has a high inductance and it is mainly carrying DC current so, the AC losses are minimal.

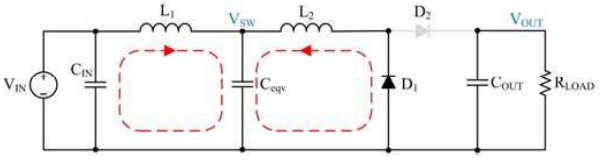
The working principle of the proposed converter is described by analyzing the steady-state waveforms of switching node voltage (V_{SW}), gate voltage (V_{GS}), and inductor under test current (I_{L2}). It is assumed that the converter perfectly operates in ZVS mode, i.e. the charge stored in the equivalent output capacitance (C_{eqv}) of M_1 is fully discharged before the FET turns on. One switching cycle can be divided into five-time sub-intervals or states as



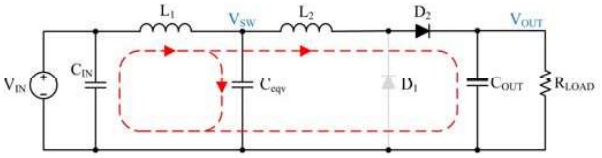
(a) State 1: M_1 ON, D_1 OFF, D_2 ON



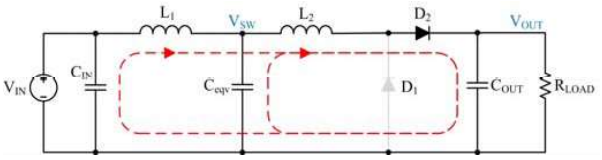
(b) State 2: M_1 ON, D_1 ON, D_2 OFF



(c) State 3: M_1 OFF, D_1 ON, D_2 OFF



(d) State 4: M_1 OFF, D_1 OFF, D_2 ON



(e) State 5: M_1 OFF, D_1 OFF, D_2 ON

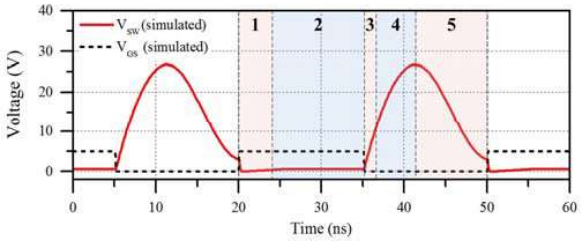
Fig. 5. Working principle of a Class E resonant boost converter is described by analyzing five states of GaN FET (M_1), Schottky diodes D_1, and D_2 corresponding to five time intervals of one switching cycle.as shown in Fig. 6. The fade color represents the off state of the device.

illustrated in Fig. 5 and Fig. 6.

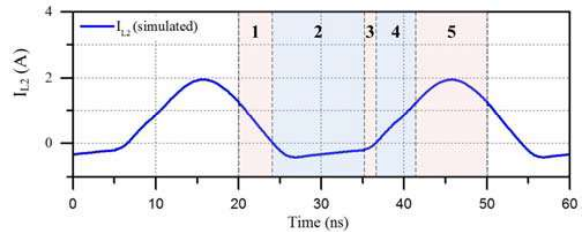
State 1: the GaN FET M_1 is turned on by the gate driver. L_1 is charged linearly from V_{IN}. L_2 is discharges through D_2 and delivers energy to the load until $I_{L2} = 0$. In ideal operation condition, it is required to switch M1 on when the drain to source voltage is 0 V to achieve soft switching.

State 2: the equivalent capacitance of D_1 is discharged through L_2. I_{L2} changes direction making D_2 reverse biased and D_1 forward biased. L_1 is still being charged by V_{IN}. During this interval, the current flowing in the GaN FET M1 is the summation of I_{L1} and I_{L2} Fig. 5.

State 3: M_1 is turned off by the gate driver. L_2 continue



(a)



(b)

Fig. 6. Simulated waveforms of (a) Voltage at switching node (V_{SW}) and gate voltage (V_{GS}), (b) inductor under test current (I_{L2}) as function of time from 0 to 60 ns i.e. 2 switching cycles at 33 MHz. A fixed load is set to be 20 Ω. One cycle is divided into five time intervals corresponding to five operation states of M_1, D_1, and D_2.

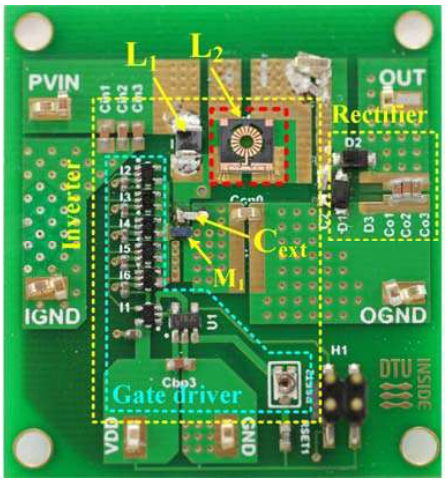
discharging through D_1 and charging the equivalent output capacitance for the GaN FET (C_{eqv}). C_{eqv} is a combination of the GaN FET output capacitance and an external ceramic capacitor in the circuit (C_{ext}). As a result, the switching node voltage (V_{SW}) is rising. By the end of interval 3, L_2 is fully discharged ($I_{L2} = 0$) and I_{L1} reaches its peak current.

State 4: D_2 is forward biased while D_1 is reverse biased. A part of the stored charge in L_1 is used to charge C_{eqv} so, V_{SW} keeps increasing. Some energy is also transferred to the load through L_2 which is charging in the same time. By the end of interval 4, C_{eqv} is fully charged and V_{SW} reaches a maximum voltage.

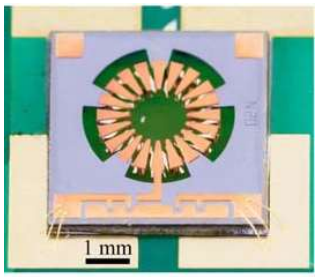
State 5: D_1 is off and D_2 is forward biased. C_{eqv} starts to discharge and its current combined with I_{L1} flows to the load. L_2 keep charging until I_{L2} reaches its peak value when V_{SW} equals V_{OUT}. L_2 then discharges through D_2 to the load until I_{L2} equals I_{L1} (C_{eqv} is fully discharged).

B. Simulation

The proposed converter topology is simulated in LT-Spice. The input voltage (V_{IN}) is set to be 8.4 V_{DC} with a fixed 20 Ω load. The simulated waveforms of the switching node (V_{SW}), GaN FET gate-to-source voltage (V_{GS}), and the inductor current (I_{L2}) are shown in Fig. 6. The switching frequency was chosen to be 33 MHz to match the peak quality factor of the MEMS air-core inductor. V_{SW} waveform indicates that the converter is operating close to ZVS mode. C_{eqv} is tuned externally to achieve ZVS operation since L_2 is fixed at 45 nH. A 180-pF external capacitor (C_{ext}) was optimized to achieve soft switching operation at 33 MHz. The choke inductor L_1 is set to a high inductance value as it is assumed to carry DC current with a small AC ripple. L_1 is chosen to be 1 µH. From the waveform of I_{L2}, the root mean square (RMS) inductor current is around 1 A with an average of 0.56 A DC. The



(a)



(b)

Fig. 7. (a) Optical image of the converter. (b) A close-up images of an air-core toroidal inductor which is mounted onto PCB by cured epoxy glue. Electrical connections are made by three 30-µm-diameter gold wires bonded in parallel.

simulated voltage conversion ratio (V_{OUT}/V_{IN}) is 1.56.

V. Experimental Results and Discussions

The proposed converter is implemented on a 4 cm x 4 cm PCB (Fig. 7). There are two main blocks corresponding to an inverter and a rectifier (Fig. 7a). A gate driver with tunable silicon oscillator is in the first inverter block. The gate driver is powered by a 5 V external voltage source. Based on simulation results, all components are selected as presented in Table I. A MEMS air-core inductor is mounted using epoxy and connected to the PCB using gold wire bonding. A magnified view of L_2 is shown in Fig. 7b. Here, the integration of L_2 is the prime interest because it is used as an energy-storage element in the resonant network. L_2 carries a high-frequency AC current, it is therefore challenging to integrate due to the excess core loss. On the other hand, L_1 is a 1-µH choke inductor that is used to block the AC current and only carries DC current. The integration of such inductors is less challenging because the unwanted high-frequency effects e.g. eddy currents, core loss, and EMI are not crucial. This allows the use of low-frequency, high-permeability magnetic materials e.g. permalloy (NiFe) and supemalloy (NiFeMo).

The measurement results are shown in Fig. 8 with the measured waveforms of gate and drain voltages. A close operation to ZVS can be observed in Fig. 8 from the

TABLE I
Component Selection

Symbol	Part number	Description
L_2	-	44.6 nH, air-core toroidal inductor
M_1	EPC8002	65 V GaN FET
L_1	LQM32PN1R0MG0L	1 µH, 1.8 A, Multilayer inductor
D_1, D_2	PMEG4010BEA	40 V, 1A, Schottky diode
C_{IN}	GRT188R61H225KE13D	2.2 µF, 50 V, X5R (quantity = 3)
C_{OUT}	GRT188R61H225KE13D	2.2 µF, 50 V, X5R (quantity = 3)
I<1:6>	74LVC1GU04GW-Q100H	Logic inverter chip (quantity = 6)
M1	LTC6905CS5	Tunable silicon oscillator
C_{ext}	GRM1885C1H181JA01D	180 pF ceramic capacitor

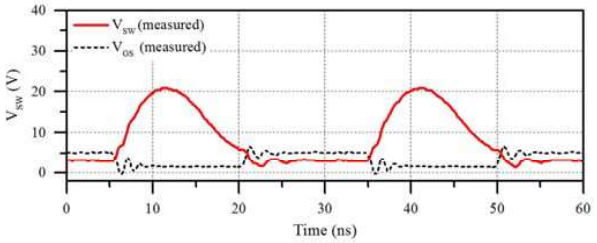


Fig. 8. Measured waveforms. (a) Voltage at switching node (V_{SW}), (b) Gate voltage (V_{GS}).

waveform of V_{SW} when V_{SW} returns to zero before M_1 is turning on. Fig. 9 shows the measured efficiency (η), power loss (P_{LOSS}), output voltage (V_{OUT}), and output power (P_{OUT}) of the converter with a sweep of input voltage (V_{IN}) from 3 V to 10 V. The average conversion ratio (V_{OUT}/V_{IN}) is 1.48. The efficiency without gate driver loss (η_{WO_GD}) increases from 73.4 % to 77.3 % with V_{IN} from 3 V to 10 V, and then saturates with an efficiency of about 77 %. The converter achieved a peak efficiency of 77.3 % at an input voltage V_{IN} = 6.5 V with an output voltage of V_{OUT} 9.7 V and an output power level of P_{OUT} = 6.1 W. The total power loss P_D is 1.5 W. The converter can delivery up to 14.5 V V_{OUT} and 10.5 W P_{OUT}. At the target switching frequency of 33 MHz, the gate driver loss is 0.15 W. The efficiency including the gate driver loss and the oscillator (η_{W_GD}) is 75.5%. For testing purposes, the gate driver is built externally, but the gate driver loss can be reduced by proper design of the gate driver with an integrated circuit process.

The MEMS inductor AC power loss was estimated via DC power loss using thermal measurement method. The idea is to drive an increasing DC current through the inductor until its thermal image is matched with its thermal image during AC converter operation. The DC power loss is obtained by multiplying the inductor voltage by the applied DC current. Fig. 10b and c show a matching of inductor temperature for the AC and DC power loss, respectively. A DC current of 1.53 A was measured with a 0.646 V DC voltage. The DC power loss is then calculated to be 0.98 W which equals to the AC power loss. In addition, the high-temperature DC resistance of the inductor is measured to be 0.42 Ω.

Fig. 10 shows thermal images of the converter with 8.4 V V_{IN}. The GaN FET temperature is 77.4 °C. Because of Cu reflects in the thermal image, an absolute thermal measurement of Cu is not possible, and the copper windings

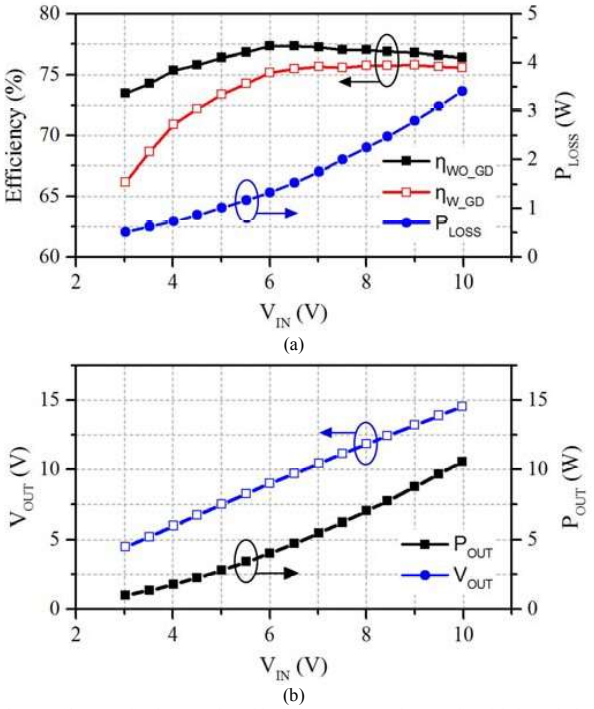


Fig. 9. Characterization results of boost converter using a microfabricated air-core inductor. (a) Efficiency of the converter without loss in gate driver (η_{WO_GD}), with loss in gate driver (η_{WO_GD}), and total power loss (P_{LOSS}) including gate driver loss of 0.15 W versus input voltage (V_{IN}). (b) Output power (P_{OUT}) and output voltage (V_{OUT}) versus V_{IN}.

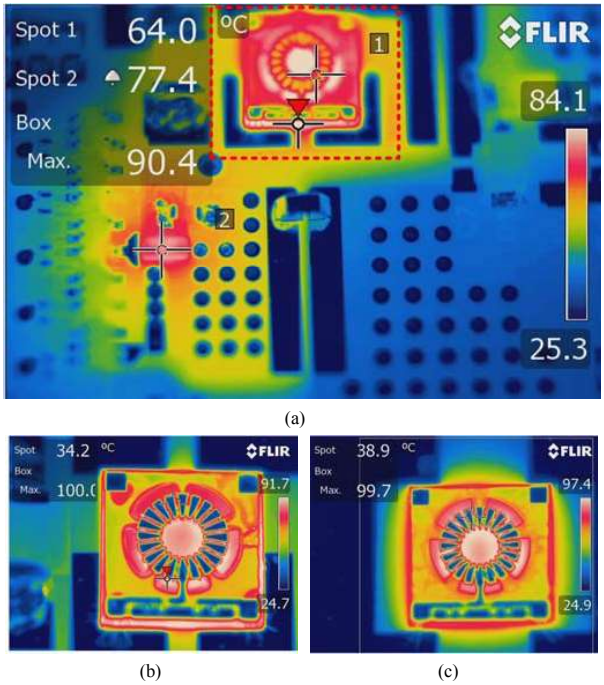


Fig. 10. (a) Thermal images of converter with V_{IN} = 8.4 V captured by FLIR camera T600 (FLIR, USA) using standard lens. Close-up thermal images of the microfabricated inductor for two cases: (b) large signal performance with AC current from the converter and (c) DC current testing with an equivalent thermal performance. DC power loss in the inductor is 0.98 W with 1.53 A DC current and 0.646 V. The close-up images were captured by a FLIR close-up IR 2.9x lens with 50 µm detector pitch. The measurement condition is with air-flow and without thermal pad for cooling down underneath the die. There is signal reflected from the board which induces biases to the measured temperature.

temperature can be estimated by matching the measured DC resistance at room temperature to the DC resistance measured at high temperature. The details of DC resistance measurement at room temperature and the method to estimate the absolute Cu temperature are presented in the Appendix. The temperature of the copper windings is calculated to 108 °C which is slightly above the temperature of the silicon die in Fig. 10b. The thermal performance of the air-core inductor can be improved by implementing a thermal pad underneath the inductor.

For better performance, the toroidal windings can be further optimized to achieve a lower resistance and a higher inductance density which will result in smaller inductors. The improvements can be made on the TSV design, e.g. increasing the diameter and the density of the circular TSVs will result in a lower resistance. Alternatively, using a single rectangular outer TSV will also increase winding coverage and lead to a lower resistance. Parallel inner TSVs will have a significant improvement in the resistance, but the effective toroidal-core volume will reduce. This can be done with a two-step deep reactive ion etching (DRIE) and electrodeposition process. A simple process modification can increase the winding thickness and density: using mold-based electrodeposition as a replacement for copper wet-etching. Mold-base technology was reported in [44] for a racetrack inductor, which has a copper thickness of 85 µm and a winding gap of 5 µm.

The heat-dissipation performance of the air-core and Si-core inductors was compared in our fabrication paper [39]. The efficiency is 64 % with the Si-core inductor and 68% with the air-core inductor with 30 °C higher than that of the air-core inductor. Indeed, the Si core has a much higher thermal conductivity for heat dissipation, but with the same windings, the air-core inductor has lower resistance compared to that of the Si-core due to: capacitive coupling and the eddy-current loss in the Si substrate. At 33 MHz, the Si-core inductor has a resistance of 1.25 Ω compared to 0.65 Ω of the air-core inductor. To further improve heat dissipation, the MEMS air-core inductor can be filled with thermal epoxy, which has a better thermal conductivity and extremely high resistivity. E.g. EPO-TEK® 921-FL (Epotek, USA) which has k = 1.1 W/mK, and $\rho > 6.\ 10^{13}$ Ωcm. We developed a screen-printing process and demonstrated an implementation of a magnetic composite core using epoxy and NiZn powders [45]. This process can also be used for making a thermal-epoxy core inductor.

VI. Conclusion

A study on silicon-embedded air-core toroidal MEMS inductor for PwrSoC applications has been presented. The proposed microfabrication process enables fabrication of 3D MEMS toroidal inductor with a unique air-core design. The inductors are embedded in a silicon substrate with through-

silicon vias and suspended copper windings. The silicon-core has been removed completely to increase the quality factor and operating frequency. Air-core and silicon-core inductors were electrically characterized and compared. The results imply that the air-core inductors are better for very high frequency operation with higher quality factor at higher frequency. The MEMS air-core inductor has a quality factor of 13.3 at 33 MHz while a silicon-core inductor has a quality factor of 9 at 20 MHz. A VHF class-E boost converter was designed and optimized for zero voltage switching using the MEMS inductor and a GaN FET. The testing results showed that the inductor can handle an RMS current of 1 A and deliver a maximum power of 10.5 W to the output with a peak efficiency of 77.3 %. Based on our results that laid the cornerstone of MEMS inductor applications in power converters, we believe that MEMS inductors will play an important role for the development and realization of the PwrSoC vision.

APPENDIX

The absolute temperature of the copper windings (T) can be estimated by a linear approximation (1) [46].

$$T = \frac{R_T/R_0 - 1}{\alpha_{Cu}} + T_0 \qquad (1)$$

where α_{Cu} = 4.29 (ppm/K) is the temperature coefficient of copper. T_0 is room temperature of 22 °C. R_T is the DC resistance measured at T °C which equals to 0.42 Ω. R_0 is the DC resistance measured at room temperature. R_0 At room temperature, the DC resistance (R_0) is re-measured precisely by applying a small DC current and measure the voltage across the inductor. An average R_0 of 0.308 Ω is measured including gold wires and PCB parasitic. The details of DC resistance measurement are presented in Table II. The absolute temperature of the copper windings (T) is calculated to be 108 °C.

TABLE II
MEASUREMENT OF DC RESISTANCE INCLUDING GOLD WIRES AND PCB PARASITICS AT ROOM TEMPERATURE

Applied DC current (mA)	Measured voltage (mV)	DC Resistance (Ω)
10.37	3.2	0.309
20.33	6.24	0.307
30.5	9.38	0.308
40.45	12.43	0.307
50.36	15.48	0.307
100.67	31.03	0.308
200.66	62.09	0.309
	Average	0.308

ACKNOWLEDGEMENT

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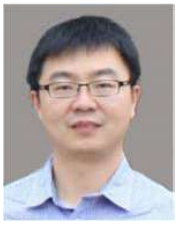

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Appendix A-J4

Hoà Thanh Le, Io Mizushima, Yasser Nour, Peter Torben Tang, Arnold Knott, Ziwei Ouyang, Flemming Jensen, and Anpan Han, "Fabrication of 3D Air-core MEMS Inductors for Very-High-Frequency Power Conversion", Journal of Microsystems & Nanoengineering, 2018.

Fabrication of 3D Air-core MEMS Inductors for High Frequency Power Electronic Applications

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ARTICLE

Fabrication of 3D air-core MEMS inductors for very-high-frequency power conversions

Hoa Thanh Le[1,2], Io Mizushima[3], Yasser Nour[2], Peter Torben Tang[3], Arnold Knott[2], Ziwei Ouyang[2], Flemming Jensen[1] and Anpan Han[1]

We report a fabrication technology for 3D air-core inductors for small footprint and very-high-frequency power conversions. Our process is scalable and highly generic for fabricating inductors with a wide range of geometries and core shapes. We demonstrate spiral, solenoid, and toroidal inductors, a toroidal transformer and inductor with advanced geometries that cannot be produced by wire winding technology. The inductors are embedded in a silicon substrate and consist of through-silicon vias and suspended windings. The inductors fabricated with 20 and 25 turns and 280-350 μm heights on 4-16 mm^2 footprints have an inductance from 34.2 to 44.6 nH and a quality factor from 10 to 13 at frequencies ranging from 30 to 72 MHz. The air-core inductors show threefold lower parasitic capacitance and up to a 140% higher-quality factor and a 230% higher-operation frequency than silicon-core inductors. A 33 MHz boost converter mounted with an air-core toroidal inductor achieves an efficiency of 68.2%, which is better than converters mounted with a Si-core inductor (64.1%). Our inductors show good thermal cycling stability, and they are mechanically stable after vibration and 2-m-drop tests.

Keywords: MEMS inductor; PwrSoC; TSVs; very high frequency; 3D

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INTRODUCTION

Inductors and transformers are the fundamental building blocks of electronics, and they are found in every electronic device. Micro-inductors and transformers (now referred to as inductors) are used in, for example, radio frequency microelectromechanical systems (RF MEMS)[1–4], microactuators[5,6], and biosensors[7]. Micro-inductors for power electronics is an emerging application in which inductors are used as energy storage elements for switched mode power supplies (SMPS). Miniaturization of SMPS has become the main focus for developing future generation power supplies, that is, power supply in package (PwrSiP) and power supply on chip (PwrSoC)[8–10]. The PwrSoC vision is to integrate all power electronics components on one chip. Higher integration lowers the cost and increases both efficiency and power density. Therefore, one of the most important inductor requirements for PwrSoC technology is the CMOS compatibility for on-chip integration. Other requirements are compact physical dimensions, a high-current capacity, and a high-quality factor for high efficiency[10]. Switching at very high frequencies (VHF, 30–300 MHz) is one route toward PwrSiP and PwrSoC[11,12]. In the VHF range, inductors with an air core or non-magnetic core are preferred, as suitable magnetic materials working at these frequencies are limited and the core implementation is very challenging[13]. For example, at 50 MHz, NiZn and CoNiZn have low magnetic saturation fluxes and cause detrimental core heating in high-flux power electronics applications[14]. In addition, VHF converters require inductance values of 10 s of nH, which is in the inductance range of air-core inductors, thereby lending themselves to a promising solution[15].

The reported MEMS inductor fabrication technologies can be classified into two main categories: on-substrate inductors and substrate-embedded inductors. To fabricate on-substrate planar inductors, surface micromachining technology has been widely used, particularly for low-aspect-ratio inductors. These methods are based on sacrificial layers[16], molding[17], or a combination of the two[18]. One method to fabricate on-substrate high-aspect-ratio 3D inductors is to use UV-LIGA lithography with SU-8 negative resist. The resist structures serve as electroplating molds and sacrificial layer[19–21] or supporting pillars[22,23] for the electrodeposition of conducting metals. The second category is embedded inductors, in which the inductors are embedded inside the Si substrate and utilize the unused substrate volume. Consequently, the inductor height above the substrate surface can be lowered, which is an advantage for integrated circuit implementation[14]. Si-embedded inductors are also an attractive solution for the advanced packaging of ultra-compact power supplies with the passive interposer[24]. There are prior-art studies of etched Si cavities for embedded inductors (wet-etched[25] and dry-etched[26]) or through-silicon vias (TSV)[24,26–28]. Yu *et al.*[26] reported a Si-embedded inductor using a fabrication process using 3D shadow masks and multiple lithographical exposures with SU-8. The interconnections are not through wafer. By contrast, TSV inductors[27] have the advantage of integrated circuit (IC) integration, that is, co-packaged or stacked systems in a package[29,30]. MEMS TSVs are known to be a promising technology for miniaturized RF MEMS and advanced system packaging and integration[31,32]. With the necessity of high-aspect-ratio TSVs for compact 3D inductors, fabrication technology for Si-embedded inductors is still a challenge.

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The near-ideal design of an air-core MEMS inductor involves free-standing windings where the remaining silicon is far from the windings because the silicon negatively affects the operation frequency and energy conversion efficiency due to parasitic capacitance (C_p) and eddy-current losses that ultimately causes undesired heating. The parasitic capacitances between the Cu windings and the Si substrate deteriorates the quality factor and decreases the operation frequency[26,33]. In addition, there is also an eddy-current loss in the Si core[34].

In this paper, we implement a fabrication process of Si-embedded 3D air-core inductors for VHF power conversion applications. The inductors are embedded in the silicon substrate, and the suspended Cu windings are secured by Si fixtures (Figure 1). Our process has three main advantages. First, the process is CMOS-compatible with a maximum processing temperature lower than 200 °C. This allows MEMS processing of CMOS electronics wafers without harming the CMOS electronics. Second, the process is highly generic and enables the fabrication of a large diversity of inductor geometries. We demonstrate the diversity by fabricating spiral, solenoid, toroid, transformer, and the 'DTU' inductor, which cannot be fabricated using wire-winding technology. The toroid geometry is especially well matched for PwrSoC applications because the magnetic field is confined in the windings to reduce EMI and minimize the cross-talk effects on other proximity electronic components[35]. Third, the TSV-based inductor technology enables the fabrication of a passive interposer with embedded 3D inductors for PwrSiP.

The paper is presented as follows: The materials and fabrication method are described with a process overview emphasizing the critical steps. Then, the fabrication and characterization results are presented. The inductors were tested with a small-signal measurement, reliability tests with thermal and mechanical shocks, and large-signal testing in VHF converters. The last section concludes the paper.

MATERIALS AND METHODS

Fabrication process overview

The fabrication process includes three main stages, 12 steps and 4 UV lithography masks (Figure 2). A 3D animation of the process is in Supplementary Video S1. We used 100-mm diameter, double-side polished, [100] crystal orientation, Si wafers. Stage 1 focuses on deep reactive ion etching (DRIE) TSV etching and begins with depositing 50-nm-thick aluminum oxide (Al_2O_3) on both wafer sides by atomic layer deposition (ALD). On the wafer front side, an Al_2O_3 hard mask is patterned by buffered hydrofluoric acid (BHF)

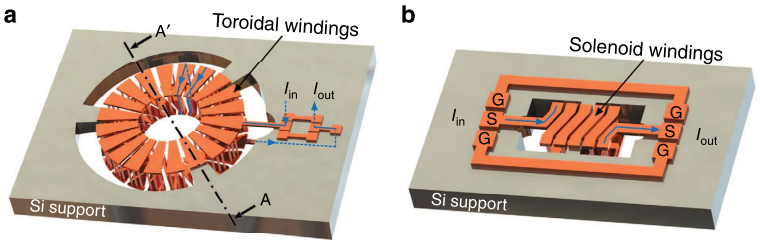

Figure 1 3D illustrations of the air-core toroidal inductor (**a**), and solenoid inductor (**b**). The input current (I_{in}) and output current (I_{out}) are indicated by the arrows. Ground-signal-ground (GSG) pads were designed for RF measurements. For the fabrication process of the cross section A′-A, see Figure 2.

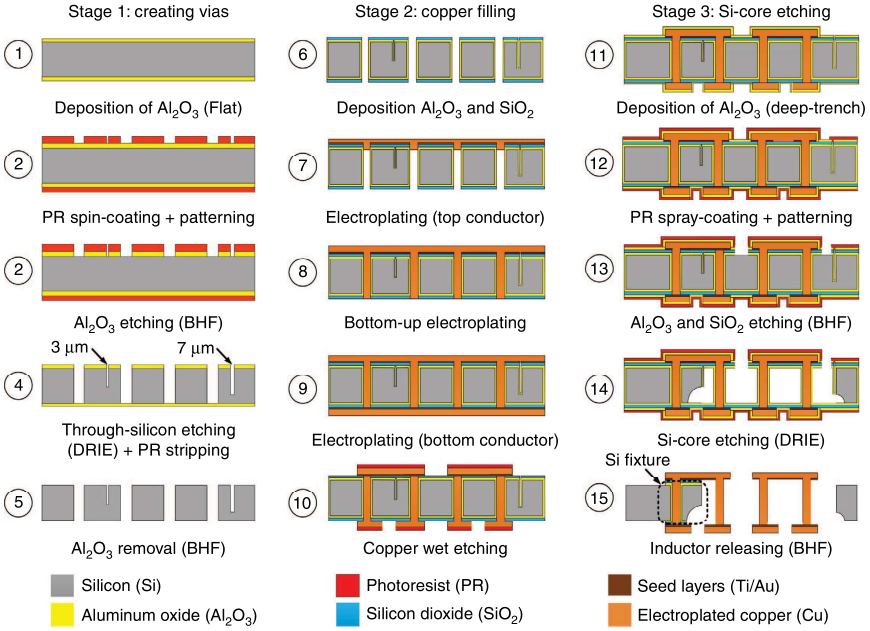

Figure 2 Cross-sectional illustration of the fabrication process flow (section A-A′ in Figure 1a). BHF, buffered hydrofluoric acid; DRIE, deep reactive ion etching.

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etch using a photoresist mask (AZ MiR 701). Next, TSVs are created by DRIE. The aspect ratio is from 9 to 12. The core shape is also defined in this step by the fixture trenches, which are between 3 μm and 7 μm wide. Finally, the remaining resist and Al_2O_3 are removed with an oxygen plasma and BHF. Stage 1 is finalized by an RCA cleaning step, which is an important preparation for stage 2.

Stage 2 focuses on creating Cu TSVs and windings. First, Al_2O_3 is deposited because it is crucial to cover and protect the deep fixture trenches (AR > 30) during the Si core removal (stage 3). Because of the high etching selectivity of Si over Al_2O_3 in an SF_6 plasma (100 000:1)[36] only 50 nm of Al_2O_3 thin film is sufficient to protect the Si support and fixtures (Figure 1b) while removing the Si core. Step 6 also includes the deposition of 1.5 μm SiO_2 by plasma-enhanced chemical deposition. It partly seals the 3-μm-wide fixture trenches to avoid defects on the top windings. Subsequently, three electroplating steps are performed to form Cu windings. We first plate a 30-μm-thick top layer and seal of the TSVs (step 7), followed by a bottom-up plating step to fill the TSVs (step 8); finally, a 30-μm-thick bottom layer (step 9) is plated. For the electroplating seed layer, we use an electron beam evaporated 10 nm Cr and 100 nm Au thin-film stack. The inductor windings are patterned by Cu wet etching using a resist mask, thus obtaining the Si-core inductor (step 10).

In stage 3, the Si core is selectively removed by inductively coupled plasma (ICP) etching. During the ICP etch, Cu is protected by a 50-nm-thick Al_2O_3 layer from the plasma environment as an additional precaution (step 11). A spray-coated photoresist uniformly covers the 30-μm-tall Cu windings and, more importantly, seals the fixture trench (step 12). The spray-coating recipe was carefully developed. Photolithography is then performed on the wafer front side, followed by BHF etching of Al_2O_3 and SiO_2 to expose the silicon (step 13) for isotropic silicon ICP etching (step 14). The Al_2O_3 layers on the fixture trenches and at the wafer backside act as an ICP etch stop, allowing complete removal of the Si core. The windings are anchored by several Si fixtures and suspended on the Al_2O_3/SiO_2 membrane. The final air-core inductor is obtained by removing the oxides in BHF.

Critical processes and process parameters

In this section, we describe the critical equipment, materials, and process parameters optimized for our process flow. We focus on the ALD of Al_2O_3 (steps 1, 6, and 11), DRIE for TSV etching (step 4), Cu electroplating for TSVs and inductor windings (steps 7–9), photoresist spray coating for BHF etching of Al_2O_3 and SiO_2 (step 12), and isotropic ICP etching of the Si core (step 14).

For steps 1, 6, and 11, a thermal ALD instrument (Picosun R200, Espoo, Finland) deposits Al_2O_3, which serves as both the DRIE etch mask and the stopping barrier. Here a 50-nm-thick Al_2O_3 film is ALD-deposited at 200 °C using alternating exposures of trimethylaluminium (TMA) (Strem Chemical, MA, USA) and H_2O. The reactor pressure was below 2 kPa during deposition. We developed two recipes for flat surface (step 1) and deep trenches (AR = 32) (steps 6 and 11), respectively. For flat wafers, one ALD reaction cycle consists of one pulse and purge step for each precursor. Together with the carrier gas (N_2), the precursor gasses are pulse injected into the reactor, and the reactor is subsequently purged with the carrier gas. The pulse time is 0.1 s, and the purge time for TMA and H_2O are 3 and 4 s, respectively. For deep trenches, the second recipe has two pulse and purge steps for each precursor. For both precursors, the first pulse is 0.1 s followed by 0.5 s of purging, whereas the second pulse is 0.1 s followed by 20 s of purging[37]. The carrier gas flow is 150 sccm and 200 sccm for the TMA and H_2O precursor, respectively. The deposition rates of both recipes are 1 Å per cycle. The thin-film thickness is measured using spectroscopic ellipsometry (M-2000V, HAWoollam, Inc., Lincoln, Nebraska, USA).

For step 4, a DRIE tool (Pegasus, SPTS, UK) etches TSVs and the fixture trenches. The etch mask stack includes 2-μm-thick MiR 701 photoresist (Microchem, Inc., USA) and a 50-nm-thick Al_2O_3 layer. The Al_2O_3 layer on the wafer back side acts as a stopping layer when etching through the Si wafer. For etching silicon TSVs and fixtures, we developed a two-segment recipe including a fast etching segment (segment A) and a notching-compensation etching segment (segment B) for the final part of the TSV. For both segments, coil powers are 2800 W and 2000 W in the etch and passivation steps, respectively. The process temperature is 20 °C for segment A and 10 °C for segment B. Segment A is used to etch 95% of Si in the wafer thickness, whereas the remainder is etched with segment B. The plasma chamber is pre-conditioned by 10 min of an oxygen plasma before DRIE of silicon. Segment A is optimized for high-speed etching with an etch rate of 11 μm min^{-1} with a 5% etch load. This recipe is based on the Bosch process with three alternating steps, including sidewall passivation (4 s, 200 sccm C_4F_8, 25 mTorr), boost (1.5 s, 350 sccm SF6, 25 mTorr, platen power 140 W), and Si etch (5 s, 550 sccm SF6, 150 mTorr). Segment B uses a low-frequency platen generator (380 KHz) to minimize notching[38] at the Al_2O_3 stop layer. The two main steps are Si etching (3 s, 400 sccm SF_6 and 40 sccm O_2) and passivation (2 s, 250 sccm C_4F_8).

For steps 7–9, electroplating is used to deposit Cu as the conductor material. It is done in a custom-designed chemical bath and setup[39]. Briefly, the electroplating bath consists of two titanium bars holding a Cu anode and a cathode, which is connected to the sample. The electrolyte contains 140 g L^{-1} $CuSO_4$, 140 g L^{-1} H_2SO_4, and 66 mg L^{-1} NaCl. Air bubbling is used for electrolyte agitation. Electroplating is performed at room temperature. Two processes are developed for, respectively, plating a 30-μm-thick Cu layer on a planar surface (steps 7 and 9) and bottom-up filling into TSVs (step 8). Dedicated wafer holders for each processes have been designed. One key feature of the holder for the first process is the stainless steel 'current thief' for excellent plating-thickness uniformity across a 100-mm wafer (< 5% peak to peak). The holder for the second process has a stainless steel plate connected to a pin to achieve electric contact from the bottom of the wafer and a plastic cover to fix the wafer and avoid plating at the edge. First, for the planar plating step, it is important to seal the TSVs to provide an electrical path for TSV filling. A pulsed current with an average current density of 2.57 A dm^{-2} is tested to be effective in closing the TSVs. Second, for TSV filling, a direct DC current at a density of 0.3 A dm^{-2} is used. A degassing step is required for both TSV closing and filling to achieve void-free Cu-filled TSVs. For degassing, the Si wafer is immersed in water and kept in vacuum (desiccator) for 10 min before abrupt venting. Trapped air bubbles expand in a vacuum and escape from cavities. This step is repeated several times until no bubbles appear, after which the wafer is mounted on the plating holder. Despite degassing, the plating process is not uniform, and some TSVs would be filled and over-plated before others. This problem is solved by removing over-plated Cu with a 'shaving' process using a stainless-steel blade. Because silicon dioxide and alumina are much harder than stainless steel, the shaving process does not scratch the sample mirror finish, which is required for subsequent processes. The filling process is then continued for the unfilled TSVs. This shaving-filling procedure is repeated several times until all TSVs are uniformly filled. More than 98% of TSVs are filled successfully with this process. Top and bottom Cu layers are then etched with a photoresist mask (AZ 4562, Microchem, Inc.) using a commercial wet etchant (APS 100, Transene, MA, USA). The etch rate is ~0.5 μm min^{-1} at room temperature.

For step 12, a spray-coating instrument (ExactaCoat, Sono Tek Co.) is used for uniform resist-layer coating of the 30-μm-tall Cu windings and, more importantly, for sealing the fixture trenches. The spray-coated resist is then used (step 12) as a mask for etching

Al_2O_3 and SiO_2 using BHF (step 13). The photoresist, AZ4562, is diluted in methyl ethyl ketone and propylene glycol monomethyl ether acetate with an optimized mixing ratio of 10:2:1. A two-step spray coating recipe is developed to simultaneously cover the Cu windings and seal the fixture trenches, which are 3 and 7 μm wide. The resist is sprayed twice with a 1-min waiting time at 28 °C and the following parameters: The spray nozzle is 30 mm above the substrate, moving along a meandering path at a speed of 10 mm s^{-1}. The resist dispense rate is 2500 μl min^{-1}. The distance between two spraying lines is 5 mm. The substrate temperature is kept at 28 °C. To avoid air bubbles in the resist, the resist solvents trapped in the trenches are slowly evaporated by storing the samples for 5 h at room temperature. Then, the resist is pre-exposure baked in a convection oven at 90 °C for 30 min. The resist thickness on flat areas is 6 μm. Multiple exposures (4 exposures, 10 s waiting time between exposures, and a total dosage of 420 mJ cm^{-2}) are necessary to avoid resist overheating. The sample is then developed for 300 s using AZ 351B (Microchem, Inc.) diluted in deionized water with a volume ratio of 1:5. Hard-baking is done in a convection oven at 150 °C for 30 min.

For step 14, an ICP silicon-etching tool (STS MESC Multiplex ICP, SPTS, Newport, UK) removes the silicon core and realizes the final air-core inductors. We developed a fluorine-based isotropic ICP recipe utilizing the undercut effect to etch Si in the toroidal core. The etch gasses are 230 sccm SF_6 and 23 sccm O_2. The coil power is 2800 W, and a minimal platen power of 3 W is applied for maximal isotropic etching. The etch rate of the Si core is 10 μm min^{-1}. The spray-coated resist and a 50-nm-thick Al_2O_3 stack serve as the etch mask. The wafer backside is coated by 50-nm-thick Al_2O_3 and two layers of the spray-coated resist. The Al_2O_3 layer stops the etching and prevents leaking of helium for backside substrate cooling.

RESULTS AND DISCUSSION

Fabrication results

We successfully fabricated 3D air-core inductors. Scanning electron microscopy (SEM) micrographs show toroidal inductors, solenoids, spirals, and a 1:1 transformer (Figure 3). In addition, we can also create inductors with arbitrary shapes; this is demonstrated by the 'DTU' inductor. The process achieved a yield of 64–95% (Supplementary Figure S4).

In this study, we fabricated 15 different toroidal inductor designs with footprints from 4 mm^2 to 16 mm^2, an outer radius (R_o) from 0.5 mm to 2 mm, and an inner radius (R_i) from 0.5 to 1 mm. The number of turns varies from 15 to 35 turns. Inductors with 30-μm-diameter TSVs were realized on 280-μm-thick and 350-μm-thick Si substrates. Thicker substrates can also be used with our process. We created inductors on a 500-μm-thick substrate with 50-μm TSVs. The inductors were designed with several TSVs in the outer ring to enhance volume coverage and minimize resistance. In addition, the identical diameter of TSVs achieves a uniform through-wafer etching and Cu TSV filling. As described before, the Si core has been removed to realize the desired air-core and suspended windings structure. The release process includes BHF dipping, deionized water rinsing, and gentle nitrogen gas drying. After the release, we did not observe any deformation of the windings. The inductors are suspended on the Si support and secured by symmetrically placed Si fixtures. Our inductors are made of only Si and Cu; no polymers (for example, PDMS or SU-8) are used. We expect the inductors to have good thermal stability, and low stresses are anticipated due to the lower thermal expansion coefficient (CTE) mismatch between Cu and Si ($\Delta_{CTE\ Cu\text{-}Si} = 14.1$ ppm per °C), compared with Cu and SU-8 ($\Delta_{CTE\ Cu\text{-}SU\text{-}8} = 35.3$ ppm per °C). The inductor windings are free hanging and only secured in the Si fixtures. Only at the fixtures, there may be higher stress due to the direct Si-Cu contact. To

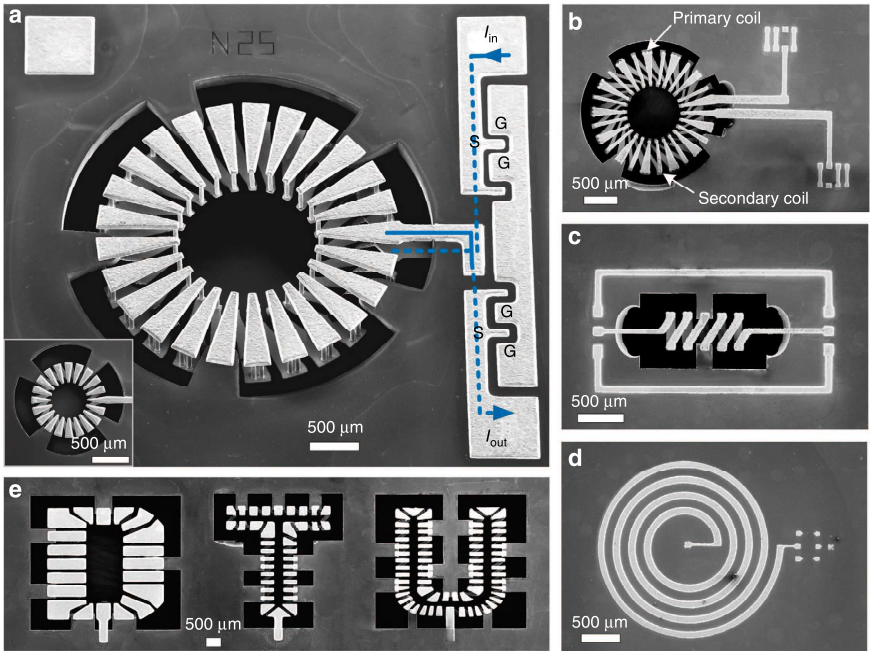

Figure 3 SEM micrographs of the fabricated 3D air-core MEMS inductors, (**a**) toroidal inductors with 16 mm^2 (1.5 mm outer radius, 0.75 mm inner radius, and 25 turns) and 4 mm^2 footprint (inset). Presented by the lines and arrows, the current flows from the top wire bonding pad, through the TSV interconnects, then passes through the windings and exits at the lower pad. The measurement pads are designed in a ground-signal-ground configuration at both terminals for wafer-level probing. Four 800 μm by 800 μm pads at the corners are for flip-chip bonding. (**b**) 1:1 toroidal transformer. The primary coil has larger conductors than that of the secondary coil. (**c**) Solenoid inductor, (**d**) spiral inductor, (**e**) 'DTU' inductor. SEM, scanning electron microscopy; MEMS, microelectromechanical systems; TSV, through-silicon vias.

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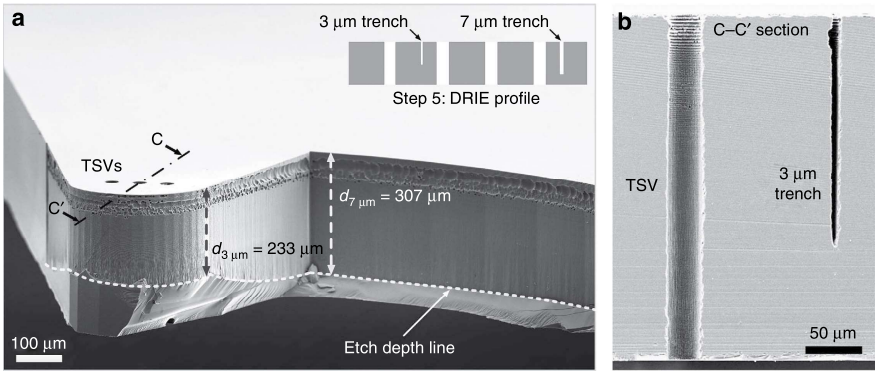

Figure 4 Etching profile after DRIE (step 5). (**a**) An SEM micrograph of a cleaved Si wafer showing the etching profile at the Si fixture. Enclosed in the fixture are three TSVs that have been etched through. As depicted in the inset taken from the process flow, the fixture trenches are etched with shallower depths of 233 and 307 μm for the 3- and 7-μm-wide fixture trenches, respectively. (**b**) A cross-sectional SEM micrograph (C-C′ direction) of the TSV and 3-μm-wide trench. This sample was cut with a diamond blade. DRIE, deep reactive ion etching; SEM, scanning electron microscopy; TSV, through-silicon vias.

enable post processing of CMOS wafers, we kept all process temperatures below 200 °C.

In the following, the fabrication results of each step are presented and discussed. Design considerations and technology challenges are described.

DRIE etching

We created the TSVs and fixture trench by DRIE (step 4). The Si fixture is designed taking advantage of the loading effects and the aspect ratio dependent etch (ARDE) effect[40], which means that wider patterns are etched with deeper than narrower patterns as presented in the inset of Figure 4a. Figure 4a shows a tilted view of the Si fixture trench after through-wafer etching. Figure 4b shows that the TSVs have been etched through while the narrow fixture trench is not. The fixture trench has 3- and 7-μm-wide sections. The 7-μm-wide trench defines the core shape, and the 3-μm-wide trench defines the shape of the Si fixture. The semicircle trench must be 3-μm wide to avoid defects that are transferred to the top inductor windings during copper plating. Illustrated by the dashed line in Figure 4a, the ARDE leads to an etch depth of 307 μm for the 7-μm-wide section and a 233-μm etch depth for the 3-μm-wide section.

Copper electroplating and wet etching

After the first plating step of a 32-μm-thick top Cu layer (step 7), the 30-μm-diameter TSVs were completely closed (Figure 5a). Approximately 35 μm of copper was deposited into the TSVs (Figure 5a, inset). Without any voids or trapped air, the TSVs were filled in the second plating process (step 8, Figure 5b). While we completely filled the TSVs directly in the second plating step, another fabrication method is to make hollow TSVs with seed layers covered uniformly on the TSVs sidewalls followed by electroplating. ALD is a suitable technique to uniformly deposit seed layers on high-aspect-ratio TSVs[41,42]. However, hollow TSVs are limited in current handling capability and are less suitable for power electronic applications. We patterned the inductor windings by Cu wet etching with a photoresist mask. Due to undercutting of the isotropic Cu wet etching, we must consider etch compensations on the mask design, meaning that, for example, a winding gap (G_w) of 94 μm requires a mask design width of 40 μm (Figure 5c). Because of the isotropic etching profile, the pitch between nearby turns is limited. To reduce the winding pitch, alternative methods are mould-based electroplating[19,20,43] and anisotropic plasma etching of Cu[44–46]. Both approaches can easily be integrated into our process with minor adaptations at steps 8 and 10.

Spray coating and Si-core isotropic dry etching

This section presents the last stage of Si-core removal to create the final air-core inductors (Figure 6). To expose the Si core to the isotropic ICP etch, photolithography is performed using a spray-coated resist. Figure 6a shows BHF etching of SiO_2 and Al_2O_3 using a spray-coated resist mask (step 13). Conformal coating of the resist is preferred, but this is impossible for the deep fixture trenches; hence, we sealed the trenches. Sprayed resist flowed into the trenches and resulted in a very thin resist layer (150 nm) on the fixture edge. This was not enough to sustain the 20-min BHF etch to remove the 50-nm-thick Al_2O_3 and 1.5-μm-thick SiO_2 because HF diffusion depends on the resist thickness. According to Fick's law of diffusion, doubling the resist thickness allows a four-times-longer etching time in BHF. Therefore, we doubled the resist thickness by developing a two-step spraying recipe, whereby the resist covers the 30-μm-tall Cu windings and seals the trenches simultaneously. After the first spraying step, the resist was optimized so that the solvents quickly evaporated (60 s) before the second spray coating, which gives a resist laying on top of the first layer and seals the trenches. The same resist thickness could be achieved with a one-step spraying recipe; however, all the resist will flow into the trenches and result in bad sealing and thin resist on the trench edges. Figure 6b shows good and poor resist trench filling and the corresponding results after Si-core etching. With poor sealing, Al_2O_3 deposited on the fixture trench sidewalls is not protected in BHF etching (step 13), resulting in an eroded fixture during the ICP Si-core etch (step 14). After Si-core etching with good trench sealing, a hollow Al_2O_3 stopping barrier remained as shown in Figure 6c.

After the inductor releasing step with BHF etching, the final air-core toroidal inductors were obtained as shown in Figure 3a. The Si core was completely removed, leaving the suspended windings secured by the symmetrically placed Si fixtures. After the ICP etch, the windings were not deformed, indicating that the residual stresses were extremely low due to the low processing temperature. We did not observe winding deformations after the release steps, indicating that the structures can withstand wet processes and that no vapor or critical-point drying steps were required. The two inductor terminals are placed on the front side for advanced packaging and characterization. We show outstanding inductor core design flexibility, and our process uniqueness is demonstrated by the 'DTU' core inductor. The

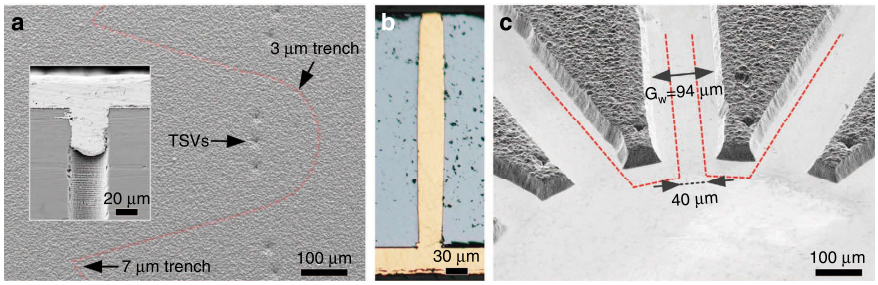

Figure 5 Cu electroplating and wet-etching results. (**a**) A top-view SEM micrograph after the first plating of the 30-μm-thick Cu layer (step 7). All TSVs and the fixture trench are closed, which provides the electrical path for bottom-up TSV filling. The transparent red line illustrates the fixture trenches that have been closed. Copper is filled 35 μm into the TSVs, as shown in the subfigure. (**b**) A void-free Cu-filled TSV after 13.5 h of plating at 0.5 A dm^{-2} (step 8). (**c**) Wet-etched toroidal Cu windings (step 9). The red lines are isotropic wet-etch compensations on the photolithography mask design. The winding pitch (G_w) is increased from the designed 40 to 94.3 μm due to the lateral undercut. SEM, scanning electron microscopy; TSV, through-silicon vias.

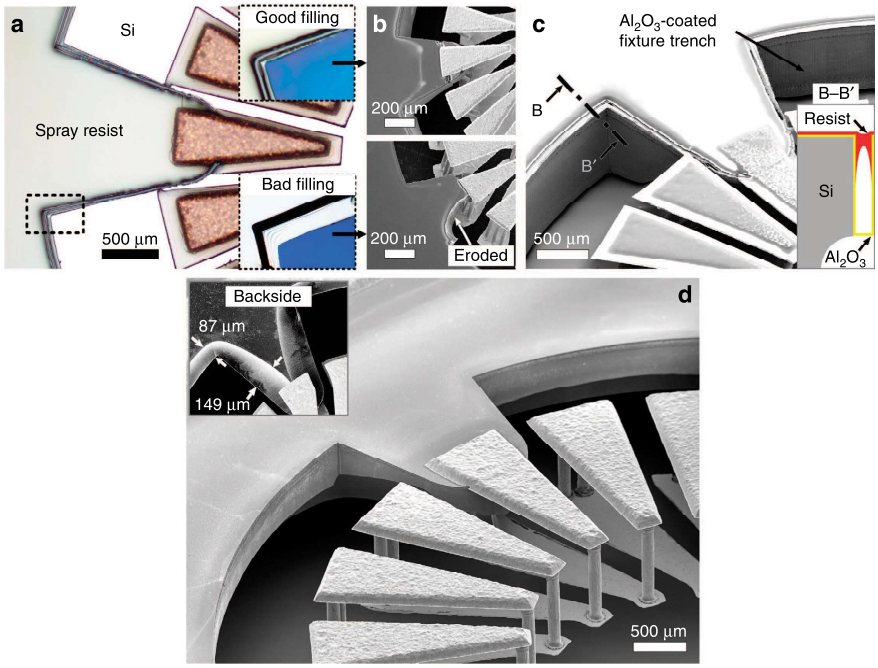

Figure 6 (**a**) Optical top-view micrograph of the patterned spray-coated resist at the Si fixture (step 12). Good and bad fixture trench resist sealing are shown in the top and bottom insets. (**b**) Si-core etching results corresponding to good and bad sealing. (**c**) A hollow Al_2O_3 stopping barrier on the fixture trench (cross section is depicted in the inset) and an Al_2O_3/SiO_2 membrane at the bottom remained after isotropic ICP Si etching. (**d**) A well-defined Si fixture was on the final inductor after the BHF releasing step, and the fixture backside is shown in the inset. BHF, buffered hydrofluoric acid; ICP, inductively coupled plasma.

other approach to remove the Si core is potassium hydroxide (KOH) Si wet etching, but the core geometries are heavily restricted, that is, square rectangular cores are possible. The KOH is, however, a cheaper batch process.

Small signal measurement

Our MEMS inductors were electrically characterized in the frequency range from 1 to 110 MHz using a precision impedance analyzer (Agilent 4294A, Agilent Technologies Inc., Santa Clara, CA, USA). The measurements were done for four toroidal inductor designs: (i) 280-μm-tall and 25-turn air-core inductors, (ii) 280-μm-tall and 20-turn air-core inductors, (iii) 350-μm-tall and 20-turn air-core inductors, and (iv) 280-μm-tall and 20-turn Si-core inductors. The inductors have a 0.75-mm inner radius, a 1.5-mm outer radius, and a TSV diameter of 30 μm. For each design, we measured three inductors, and for Figure 7, 12 inductors in total were measured. More details on the inductor design, modeling, and measurement will be presented in our upcoming paper.

Figure 7a shows the measurement results for three inductors of design (i). The measured inductance and resistance values are 20% larger than simplified analytical calculations of ideal toroid inductors. At the peak quality factor (Q) frequency (41.2 MHz), the inductance is 34.3 nH ± 0.12 nH, and Q is 12.9 ± 0.17. The resistance is 180 ± 7 mΩ at 1 MHz. The inductors were from the same wafer. For all measurement points, the average peak-to-peak variations are 0.56% (inductance), 2.67% (quality factor), and 2.56% (resistance), respectively. We have also compared the inductors from two different process runs. Ten toroidal inductors with 280 μm thick and 20 turns were measured. The standard

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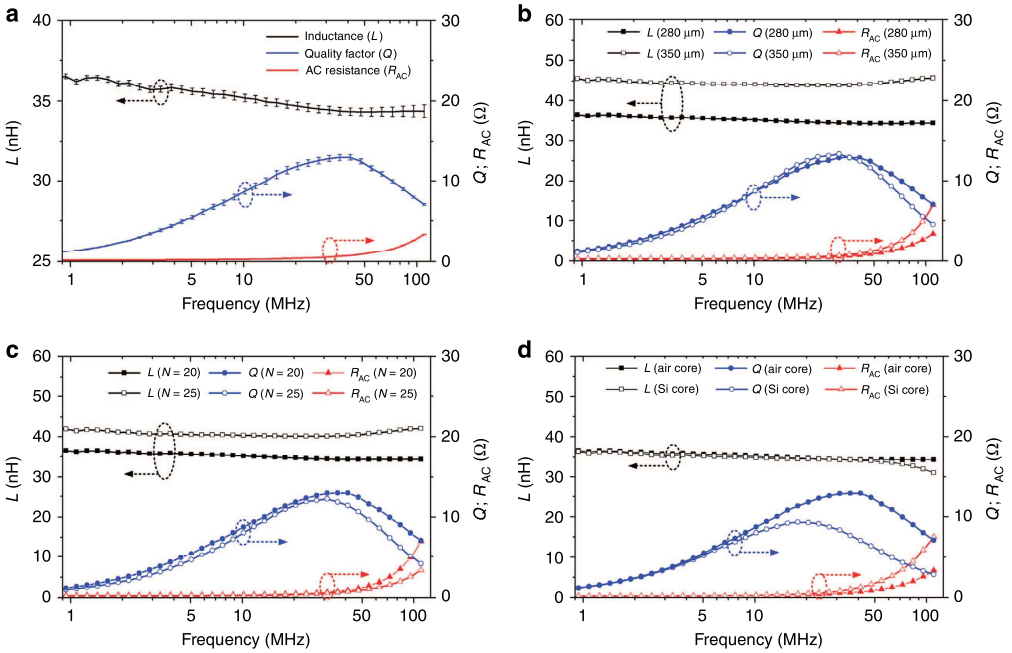

Figure 7 Comparison of the frequency-dependent inductance (*L*), quality factor (*Q*), and AC resistance (R_{AC}) of selected toroidal inductors designs. (**a**) Measurement of three inductors with the same design (280-μm tall, 20-turn air-core toroidal inductor). The mean values and error bars are plotted. (**b**) Comparing 20-turn air-core inductors fabricated using 280- and 350-μm-thick substrates. (**c**) Comparing air-core inductors with 20 and 25 turns. (**d**) Comparing air-core and Si-core inductors.

Table 1 Comparison of the electrical performance of embedded air-core toroidal inductors

Inductor from	R_{DC} (mΩ)	$L_{density}$ (nH mm^{-3})	Q_{peak}@frequency (MHz)
This work (toroid)	180–263	13.6–17.3	10–12.9@31.8–72.6 MHz
Yu *et al.*[26] (toroid)	400	3.12–4.16	16–17.5@40–70
Li *et al.*[28] (toroid)	265	2.95	10.5@14

deviations are less than 1.9% for inductance, 8.4% for resistance, and 9.2% for quality factor. The inductance tolerance of our inductor is lower than that of the wire-wound inductors (5–10 %). The relatively small variations indicate that the fabrication process is reproducible. This is an essential advantage for SMPS and electronic design.

For PwrSoC inductors, a high inductance and a high Q factor are desired. For a toroidal inductor, this could be done by increasing the inductor height or number of turns. We compared 350 to 280-μm-tall inductors and 25 to 20-turn inductors. The results are shown in Figures 7b and c. Our data show that there are tradeoffs between the inductance density, Q-factor, and optimal operation frequency. By increasing the number of turns, a higher inductance density (17.3 nH mm^{-3}) is achieved, however at the same time causing a lower peak Q-factor (10) at a lower frequency (31.8 MHz). Taller inductors show a higher Q-factor at higher frequencies, whereas the inductance density is lower (14.2 nH mm^{-3}).

Figure 7d compares air-core and Si-core toroidal inductors fabricated with 20 turns on a 280-μm-thick wafer. Air-core inductors showed a 140% higher-quality factor and a 230% higher-operation frequency than did the Si-core inductors (Q of 9.3 at 17.8 MHz). At high frequencies (> 50 MHz), the inductance decreases and the resistance increases due to the increased parasitic capacitances (C_p) and the eddy-current losses in the Si core. C_p was measured to 3.71 pF and 11.5 pF for the air core and the Si core, respectively. A higher C_p increases the effective resistance with increasing frequency. Therefore, without removing the Si-core, $R_{AC\text{-}eff}$ is 108 and 140% higher than that of the air-core inductor at 50 and 100 MHz, respectively. We also fabricated inductors that can operate at a higher frequency of 72.6 MHz with a Q of 11.5 and an L of 42.5 nH. This inductor (350-μm-tall, 5 mm^2) has a lower parasitic capacitance due to 20 times smaller pads (Figure 1a), compared with that of the inductor in Figure 3a.

Table 1 compares the electrical performance of our MEMS toroidal inductors and prior art on embedded inductors. Our inductors have four-times-higher inductance density compared to other Si-embedded toroidal inductors with typical densities of 3–4 nH mm^{-3}. This is because our high-aspect-ratio TSVs enable compact inductors to be embedded in a Si wafer for a decreased total volume and higher inductance density. Our inductor DC resistance is lower while the Q-factor is similar to the previous work.

Thermal and mechanical reliability

Our 3D MEMS toroidal inductors were tested with thermal shock and drop testing experiments. First, the thermal shock test was performed in a temperature shock test chamber VT 7010 S2 (Vötsch, Weiss Technik UK Loughborough, Leicestershire, UK). The temperature was rapidly cycled from −40 to 150 °C under vacuum

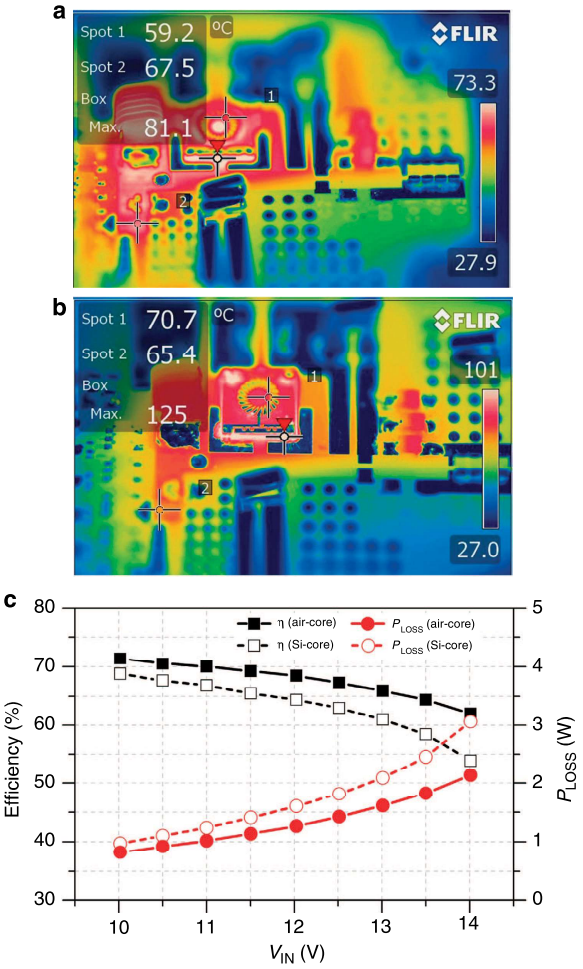

Figure 8 Thermal images of the converter ($V_{IN} = 12$ V) with (**a**) the air-core inductor and (**b**) the Si-core inductor. The images were captured by FLIR camera T600 (FLIR, USA) using a standard lens. (**c**) The efficiency and the converter power loss are presented as a function of the input voltage (V_{IN}) for the air-core inductor and the Si-core inductor.

for 250 cycles. The heating rate was 3 °C min^{-1}, and the cooling rate was 3.5 °C min^{-1}. We tested eight inductors: four air-core inductors (TSV diameters of 30 and 50 µm) and four Si-core inductors (TSV diameters of 30 and 50 µm). After 250 cycles, the inductors were optically inspected and electrically characterized. All inductors were electrically functional, and no deformation or cracks were observed. More details of the testing results can be found in Supplementary Figures S1 and S2.

Second, drop testing experiments were conducted to probe the mechanical stability of the suspended windings. The inductors were mounted on a PCB test board, which then was dropped on an aluminum plate from a height of 0.5, 1, and 2 m. Up to the height of 2 m, no winding deformation was observed, and the electrical properties were unchanged. Our results suggest that the fabricated inductors are stable for practical use in electronic circuits. The optical images of tested inductors are shown in Supplementary Figure S3. For applications that require more robust windings, we suggest filling the air core with epoxy or silicon rubber. We anticipate a slight decrease in performance.

Large signal testing in VHF converters

The large signal performances of our air-core toroidal inductors and Si-core toroidal inductors were compared in a 33 MHz class E resonant DC-DC boost converter (Figure 8). More details about the converter design are in Ref. Le HT, Nour Y, Han A, et al. Microfabricated air-core toroidal inductor in very high frequency power converters, unpublished observations. The input voltage ranges from 10.0 to 14.0 V_{DC}, the output voltage ranges from 25.5 to 35.4 V_{DC}, and the output power ranges from 1.6 to 3.2 W. Figures 8a and b show thermal images of the converter with an input voltage of 12.0 V and an output voltage of 30.0 V. Our Si-core inductor shows a maximum temperature of 125 °C, a power converter efficiency (η) of 64.1%, and a converter power loss (P_{LOSS}) of 1.6 W. In contrast with the Si-core inductor, our air-core inductor shows a significantly lower peak temperature of 85 °C, a higher converter efficiency (68.2%), and a lower converter power loss (1.26 W). As the inductor geometries are identical, our results imply that the Si core causes a power loss of 0.34 W for the converter, which results in an additional 40 °C temperature increase. This is consistent with our small signal resistance measurements; at 33 MHz, the Si-core inductor has a higher resistance (1 Ω) than the air-core inductor (0.6 Ω). The increased resistance is due to the capacitive and the eddy-current loss in the Si core.

CONCLUSION

We successfully realized 3D air-core MEMS inductors for VHF power electronic applications. Compared with prior art on toroid inductors, we demonstrated a fourfold larger inductance density while keeping a good-quality factor and operation frequency. We have demonstrated that the proposed process is CMOS-compatible for the post integration of 3D inductors and highly generic for fabricating a large diversity of inductor geometries, for example, a spiral, solenoid, and toroidal inductor; a toroidal transformer; and a 'DTU' inductor. Our small-signal and large-signal measurements show that the air-core inductors outperform the silicon core inductors in the MHz regime. Our technology of integrated 3D inductors with high-aspect-ratio TSVs has a great potential for PwrSiP as an advanced passive interposer with the embedded 3D inductors. In the next step, we will focus on integrating magnetic materials as the core material, to expand the frequency range in which the inductor can be used. While our technology has been developed for power systems on chip (PwrSoC) applications, we believe that our generic technology will find other applications, for example, integrated high-Q LC filters may be used in RF MEMS for transmitters and receivers.

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COMPETING INTERESTS

The authors declare no conflict of interest.

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Supplementary Information for this article can be found on the *Microsystems & Nanoengineering* website (http://www.nature.com/micronano)

Appendix A-C1

Yasser Nour, Arnold Knott, Ivan H. H. Jørgensen, "Investigating Enhancement Mode Gallium Nitride Power FETs in High Voltage, High Frequency Soft Switching Converters," in IEEE International Conference on Power electronics, machines and drives (PEMD), Glasgow, Scotland, 2016.

Investigating Enhancement Mode Gallium Nitride Power FETs in High Voltage, High Frequency Soft Switching Converters

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Investigating Enhancement Mode Gallium Nitride Power FETs in High Voltage, High Frequency Soft Switching Converters

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Keywords: Gallium Nitride, Soft Switching, ZVS Buck.

Abstract

An increased attention has been detected to develop smaller and lighter high voltage power converters in the range of 50V to 400V domain. The main applications for these converters are mainly focused for Power over Ethernet (PoE), LED lighting and AC adapters. This work will discuss a study of using enhancement mode gallium nitride switches to form a 50V quasi-square-wave zero-voltage-switching buck converter running at 2-6 MHz under full load. The designed converter achieved 83% efficiency converting 50V input voltage to 12.2V at 9W load.

1 Introduction

The demand for smaller size and lighter weight power converters has led the development of higher switching frequency converters. With silicon MOSFETs reaching its performance limits [1], new routes for research have led to achieve switching at high frequency (3MHz - 30MHz) and above [2, 3, 4, 5, 6, 7]. These routes are new semiconductor materials, innovative packaging, and converter topologies in addition to high frequency passives development.
Operating at high frequencies enables the integration of the magnetic components and other passive elements achieving higher power densities [8]. For high input voltage converters, operating at high frequency should be combined with a kind of soft switching techniques to avoid excess power losses which can lead to converter thermal run-away. For sake of integrating and increasing the power densities to higher levels, wide bandgap materials provided the needed switching performance.
It has been reported by many researchers that gallium nitride (GaN) devices has promising figure of merits (FOM). The theoretical lateral devices on-resistance of the MOSFET times the gate charge of GaN was reported in Figure.1 which shows the superiority of GaN HEMT for two different feature sizes especially at higher breakdown voltages [9].
This paper investigates the advantages and requirements of using enhancement mode gallium nitride (eGaN) based switches in a high frequency high voltage power converter.

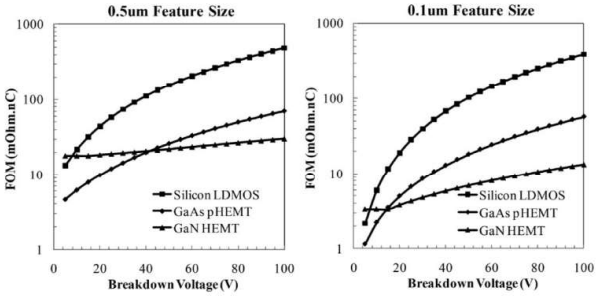


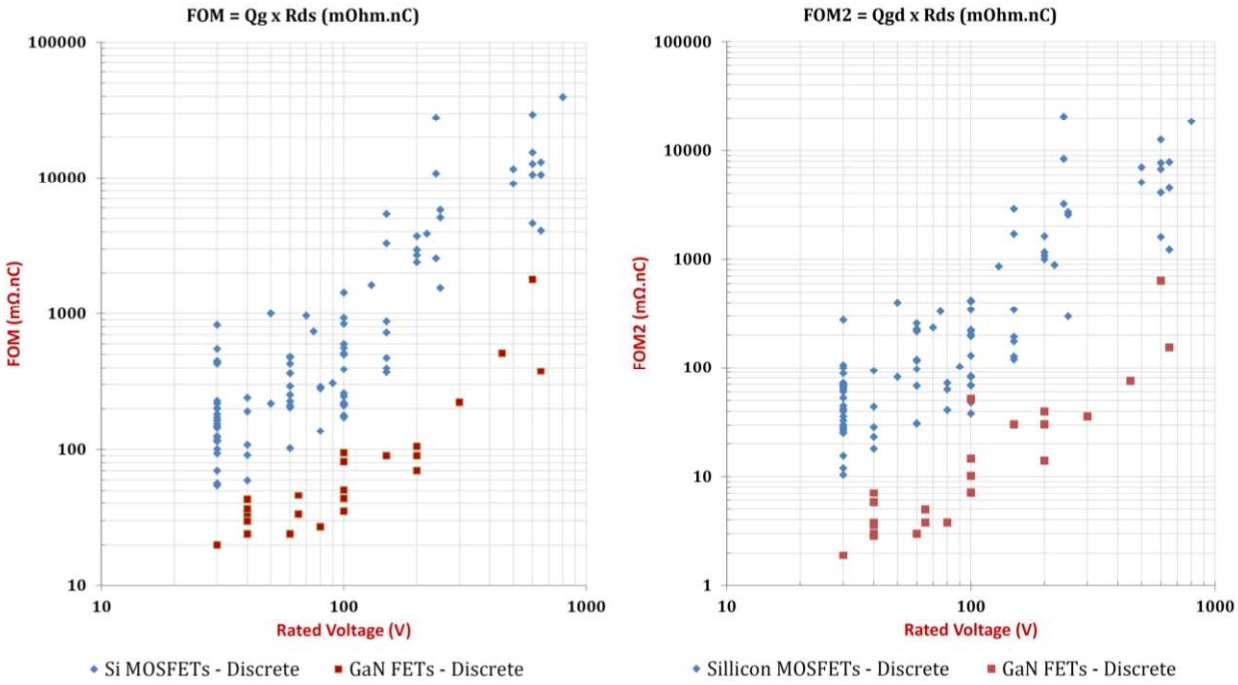
Figure 1: Analytical FOM of lateral power switches: Si NMOS, GaAs pHEMT, and GaN HEMT for two minimum feature sizes [9]

2 Gallium Nitride Versus Silicon

Gallium nitride has a higher bandgap and electron mobility compared to silicon, silicon carbide and gallium arsenide which make gallium nitride the preferred material for this research [3]. GaN FETs have a potential for development. It is more expensive than silicon counterparts but with designs shift towards using them will reduce the price and hopefully enables more integration into the same die. The authors collected FETs parameters to compart the figure of merits for silicon switches and GaN switches. The results were collected from more than 140 MOSFET datasheets.
The first figure of merit represents the on-resistance of the switch times the total gate charge is shown in figure 2a. The resulting graph shows the superiority of GaN devices over silicon devices and the gap increases as high as the breakdown voltage goes.
Figure 2b shows a second figure of merits graphed against maximum drain to source voltage. The second FOM represents the gate to drain charge times the on-resistance of the switch. The figure also shows better GaN performance compared to silicon.

3 Theory of QSW-ZVS Buck Converter

The most basic step down switching converter is the buck converter. The buck converter can operate in a continuous-



a. summary of high voltage FETs $Q_{gtot}.R_{ON}$ b. summary of high voltage FETs $Q_{gd}.R_{ON}$

Figure 2: Summary of gallium nitride FETs vs. silicon MOSFETs figure of merits

conduction mode (CCM) or in a discontinuous conduction mode (DCM), depending on the waveform of the inductor current. In CCM, the inductor current flows during the entire cycle, whereas in DCM the inductor current flows only during part of the cycle. In DCM, it falls to zero and remains at zero for some time interval, before it starts to rise again in the next cycle. Operation at the boundary between CCM and DCM is called the critical conduction mode as shown in figure.3. For synchronous buck converter, which uses two switches to chop the input DC voltage, the inductor current will be continuous even if it falls under zero as a result of using bidirectional switches [10].

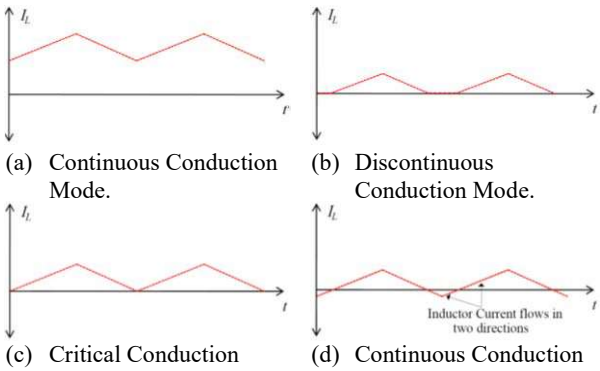
Zero-Voltage-Switching Quasi-Square-Wave (ZVS-QSW) is a switching technique which uses the current passing through a switch to charge or discharge the output capacitance of a semiconductor switch resulting in much lower output capacitance related switching losses [2, 7]. ZVS technique is based on turning-on the power MOSFET switches when the drain to source voltage drops to zero volt (i.e. V_{DS} = 0) to mitigate the switching and diode reverse recovery losses. ZVS-QSW is the simplest technique used to achieve soft switching by simply reducing the output inductance L_O under the critical value and using bi-directional switches to avoid main current discontinuity. QSW-ZVS buck converter can be realized by designing the inductor value to be less than the inductor value needed to operate a buck converter in critical conduction mode which is given by Equation.1 [10].

$$L_{O(min)} = \frac{(1-D)}{2F_{SW}} R_{Load} \quad (1)$$

For QSW-ZVS operation, it is important to assure the inductor current has the needed negative valley value based on equation.2 [10].

$$I_{Lo\,(min)} = I_{Load} - \frac{\Delta I_{Lo}}{2} = \frac{V_O}{R_{Load}} - \frac{V_O}{2L_O F_{SW}}(1-D) \quad (2)$$

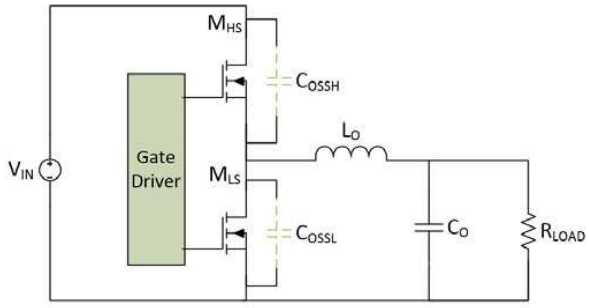
Accurate gate drive timing is needed to achieve zero voltage switching and also to reduce the power loss in body diodes or power loss due to reverse conduction charge [10, 11]. Simple QSW-ZVS buck converter and ideal waveforms are shown in Figure.4.



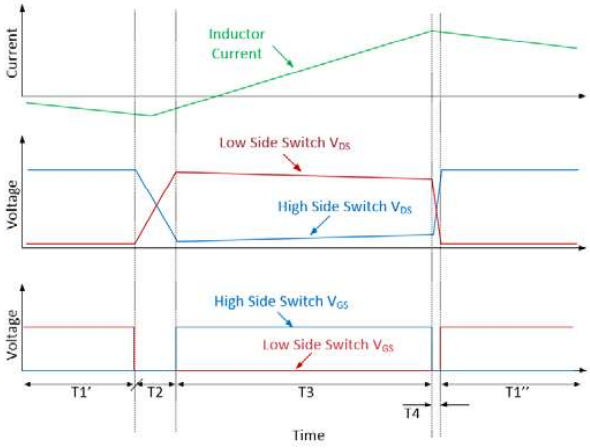
(a) Continuous Conduction Mode. (b) Discontinuous Conduction Mode.

(c) Critical Conduction Mode. (d) Continuous Conduction Mode Using Bidirectional Switches.

Figure 3: Basic Buck Converter Modes of Operation [10].



(a) Power stage schematic.



(b) Converter waveforms at heavy load.

Figure 4: Simple QSW-ZVS Buck Converter

To understand how QSW-ZVS buck converter works in steady state, the switching period -which is shown in figure 4b- was divided into four sub-periods [11].

a. Sub-Period 1 [T1' and T1"]:
In this sub-period, the low side switch is fully ON and the high side switch is OFF. The switching node voltage equals the voltage drop across the low side switch. The inductor current is decreasing less than zero at this period.

b. Sub-Period 2 [T2]:
This sub-period starts when the duty cycle signal forces the low side switch to turn off. The voltage across the low side switch starts to rise due to the negative inductor current is charging its output capacitance and the voltage across the higher side switch is falling to zero. When the voltage across the high side switch reaches zero, the high side driver turns the high side switch on.

c. Sub-Period 3 [T3]:
In this sub-period, the low side switch is OFF and the upper side switch is ON. The switching node voltage is equal to the voltage drop across the high side switch subtracted from the input Voltage. The inductor current is rising to its maximum value at the end of duty cycle.

d. Sub-Period 4 [T4]:
This sub-period starts from the end of duty cycle input signal. The driver forces the high side switch to switch off. The positive direction inductor current quickly discharge the capacitances connected to the switching node. The voltage of the switch node drops to zero. When the voltage across the low side switch reaches zero, the low side driver forces the switch to be "ON".

In case of operating a ZVS-QSW converter in light load the inductor average current should be equal to the load current, and the peak and the valley of inductor current will be changed. Consequently, the slew rate of switching node will be changed based on the load current. The optimum gate signal timing should be modified to avoid shoot-through problems if short dead-time is provided and avoiding body diode losses if large dead-time is provided. If the gate signalling is not optimized, it will lead to lower obtained efficiencies.

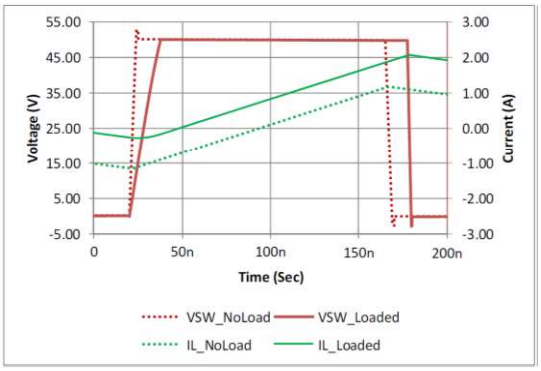
4 System Description and Simulation Results

A QSW-ZVS converter was built using 100V eGaN FETs but the input voltage was limited to 50V for this experiment. Two variants of the converter were tested at two different frequencies for investigation. With a change in the inductor and the switching frequency, a converter running at 2MHz uses a 2.2uH inductor and a 6MHz converter with 500nH air core inductor.
The two converters were simulated using a SPICE based simulation tool. Figure 5 shows the converter simulation results running at 2MHz. The inductor current and the switching node voltage have been shown the first subplot. The gate signals at no load condition have been shown in the second subplot. The third subplot shows the gate signal at full load.
It is obvious from the simulation results that the rise time and the fall time of the switching node voltage is load dependant.
The gate signalling is changed manually to give the best results.

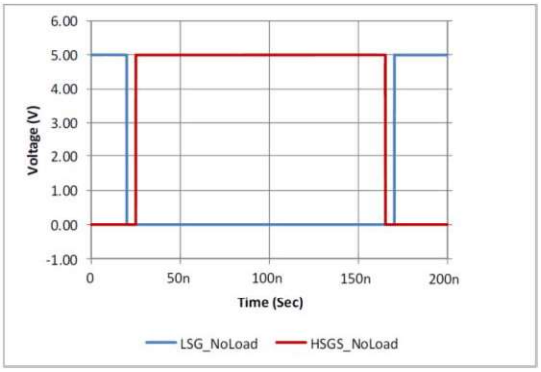
5 Experimental Setup and Results

A printed circuit board was assembled to form the power stage. The inputs for the gate driver were provided through a signal generator connected to two BNC connectors on the test board shown in figure 6. The signal generator is used to fine tune the dead time to achieve zero voltage switching.
The first converter was assembled and tested at 2MHz and using a 2.2uH inductor. Switching node and the inverse duty cycle waveforms are shown in figure 7 where the first sub-graph shows the no-load waveforms. The waveforms show some reverse conduction due to the inserted dead-time. Figure 7.b shows the waveforms at full load of 9 watts at 13.2V output voltage. The switching node waveform shows the obvious low dv/dt for the switching voltage rise time at full load.

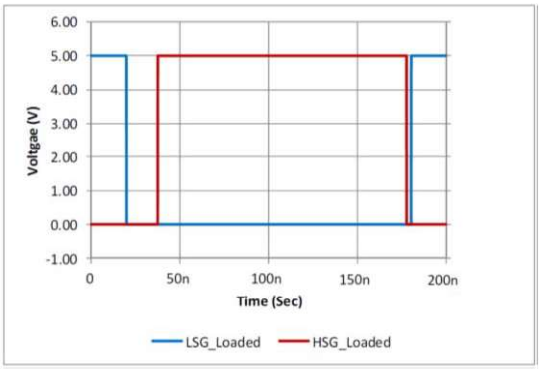
The second converter was built to switch at 6MHz and the inductor was changed to 500nH air core inductor as shown in figure 8. Figures 8.a and 8.b show the converter switching node and the inverse duty cycle of the converter running at 6MHz at no load and full load respectively.
The converter switching at 6MHz achieved 83% efficiency at full load. On the other hand the converter which is running at 2MHz achieved 75% efficiency at full load it was noted that the inductor dominated the power losses.



(a) Switching node voltage and inductor current under full load and no load conditions



(b) Gate to source voltage for high side and low side FETs at no load



(c) Gate to source voltage for high side and low side FETs at full load

Figure 5: Simulation Results of the GaN converter switching at 2 MHz

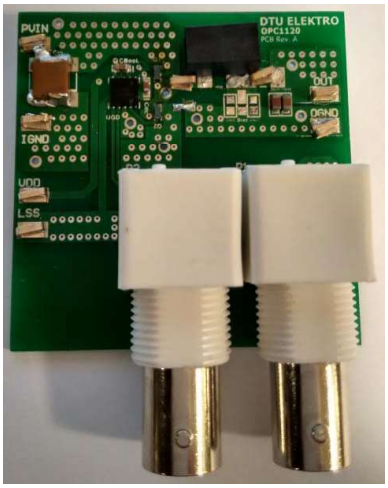
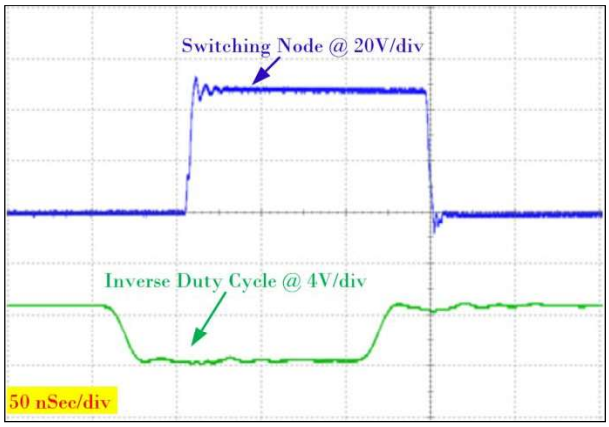
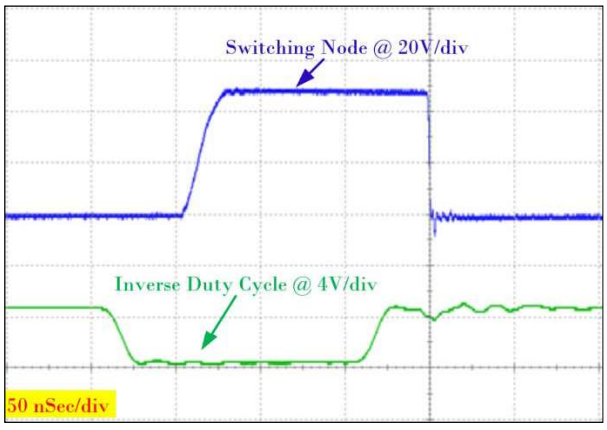


Figure 6: a Photograph of the test PCB

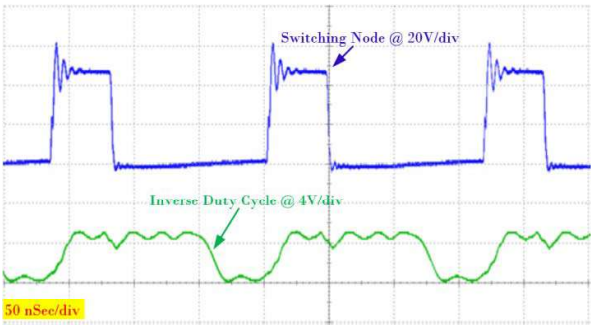


(a) No Load Condition

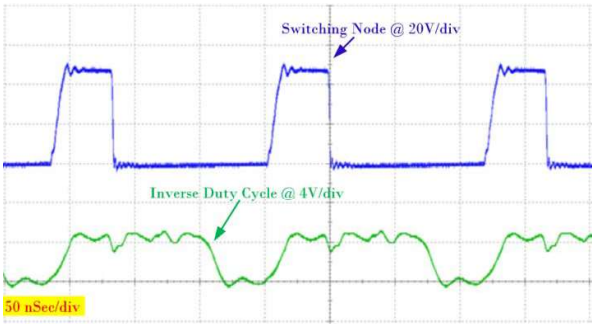


(b) Full Load Condition

Figure 7: Experimental waveforms of switching node and inverse duty cycle at 2 MHz



(a) No Load Condition



(b) Full Load Condition

Figure 8: Experimental waveforms of switching node and inverse duty cycle at 6MHz

6 Conclusion

In this study, gallium nitride devices show promising results. Gate driver and dead time should be accurately fine-tuned on-the-fly not only to achieve high efficiencies but also to prevent hard switching from happening and causing a damage to the converter. QSW-ZVS buck converter shows the capabilities to switch at much higher frequencies compared to the conventional hard switching buck converter. The converter was built using 100V eGaN FETs but the input voltage has been limited to 50V for this experiment. The converter was tested at two different frequencies for investigating the performance with a change in the inductor. The converter running at 2 MHz uses a 2.2uH inductor and the efficiency achieved is 75% at 12V, 9W output load. The low efficiency is mainly due the inductor losses. The frequency changed to 6 MHz and a 500nH air core inductor was used to form the converter. The efficiency achieved was 83%.

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Appendix A-C2

Jens Christian Hertel, Yasser Nour and Arnold Knott, "Very High Frequency Two-Port Characterization of Transistors" e-poster in International Workshop on Power Supply on Chip (PwrSoC), Madrid, Spain, 2016.

Very High Frequency Two-Port Characterization of Transistors

Authors: Jens Christian Hertel, Yasser Nour, Ivan H. H. Jørgensen & Arnold Knott

Abstract: **To properly use transistors in VHF converters, they need to be characterized under similar conditions. This research presents a two-port method, using a network analyzer (NWA) with a S-port setup. The method is a one-shot method, providing fast results of the off-state parasitics of the transistors.**

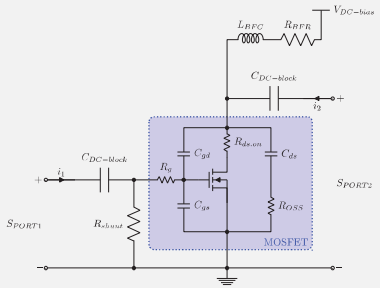

Fig 1. MOSFET in Two-port Characterization

Introduction:

- Resonant power converters are becoming more interesting for on-chip power solutions.
- As the switching frequency increases, the parasitic elements of the transistors are used as part of the circuit.
- Proper characterization is needed. The two-port solution is an interesting method, as it is a one-shot relatively easy method

Two-port theory:

- MOSFET modelled as per fig 1. [1]
- Protection circuitry implemented, blocking DC voltage on equipment [2].
- Drain-Source voltage biased through a 10mH choke (L_{BFC}) as well as a large resistance for proper AC blocking capabilities.
- Network derived through ABCD matrices.
- Formulas for capacitances and resistances, from the Z-results of a two-port S-parameter solution.
- Capacitances and Resistances are found through results of the Z-parameters:

$$Z_{C_{gs}} = \Im\left(-\frac{z_{11}z_{22} - z_{12}z_{21}}{z_{21} - z_{22}}\right) \qquad Z_{R_g} = \Re(z_{11})$$

$$Z_{C_{gd}} = \Im\left(\frac{z_{11}z_{22} - z_{12}z_{21}}{z_{21}}\right) \qquad Z_{R_{oss}} = \Re\left(\frac{1}{z_{22} \cdot C_{gd}^2 \cdot \omega^2}\right)$$

$$Z_{C_{ds}} = \Im\left(\frac{z_{11}z_{22} - z_{12}z_{21}}{z_{11} - z_{21}}\right)$$

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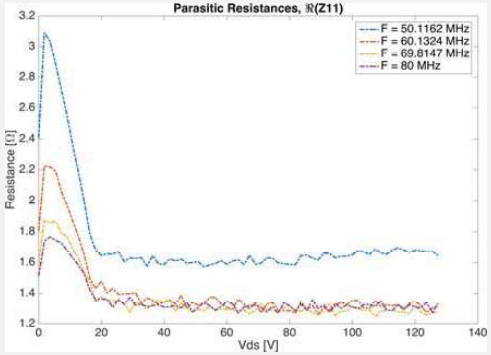
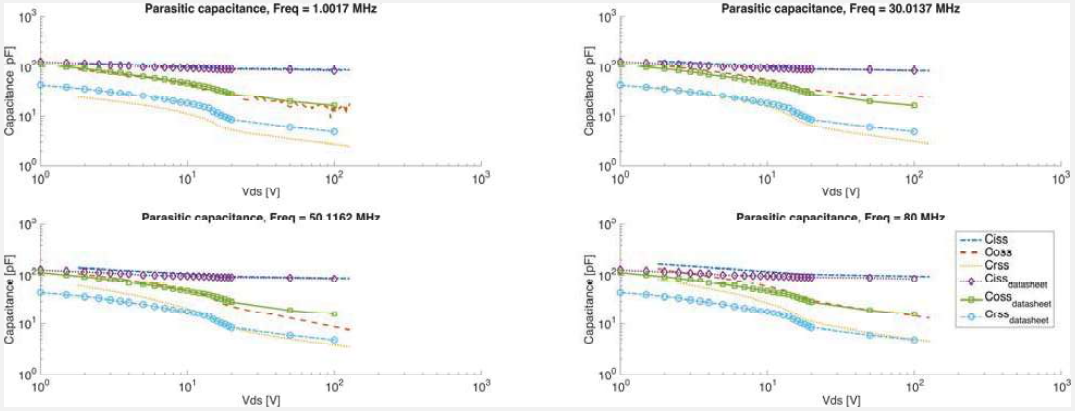
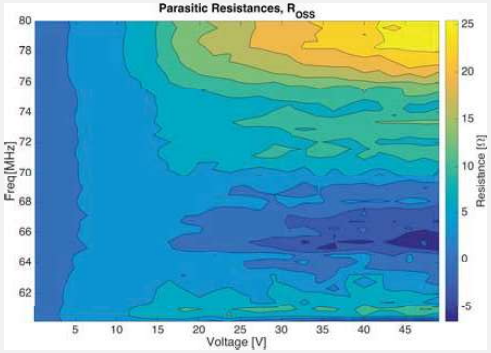
Conclusion: The two-port S-parameter measurements is advantageous to the one-port measurement, as it is a one-shot measurement. The two-port results matches the datasheet values on capacitances. Resistance values are similarly within range of expectation. However, R_{oss} measurements should be confirmed with a one port setup. Future work also consist of including this in a loss model simulation and measurements in a VHF converter.







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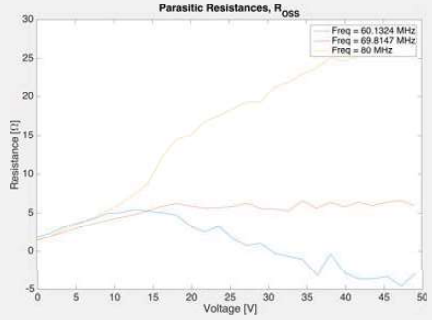
Additional results: Looking at contour plots of the capacitance reveals interesting things:

- C_{RSS} and C_{OSS} are stable over frequency.
- C_{ISS} increase with frequency. However, effect most notably over voltage.
- Measurement setup seems to have an unwanted effect around 30-40 MHz. Corresponds to unknown inductance in the measurement setup.



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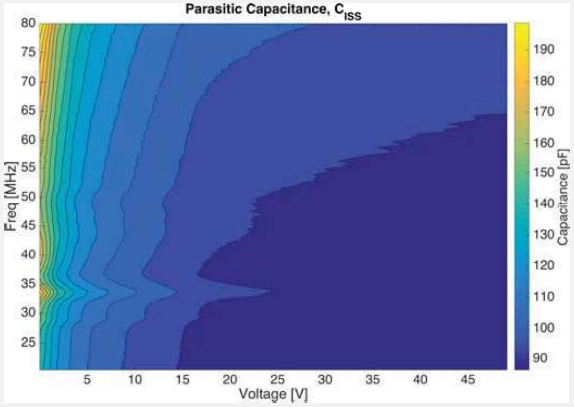
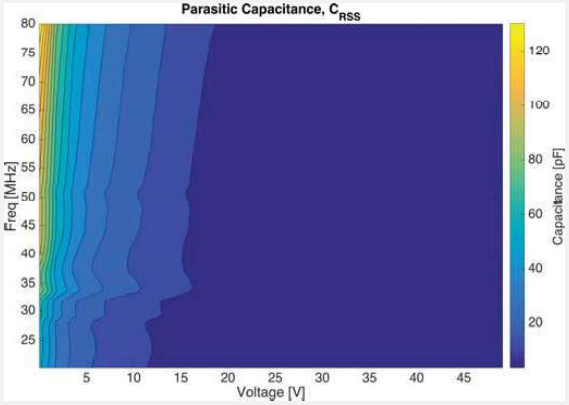
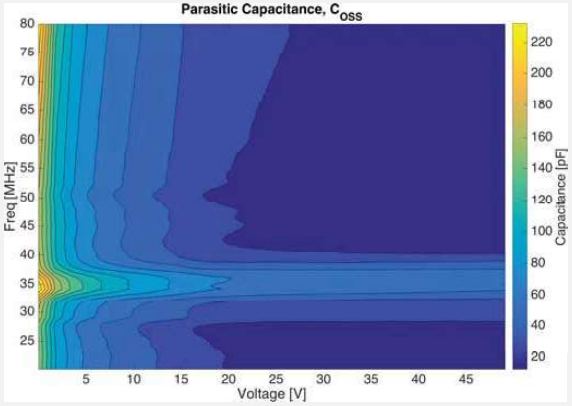
[1] A. D. Sagneri, D. I. Anderson, and D. J. Perreault, "Optimization of transistors for very high frequency dc-dc converters," *2009 IEEE Energy Conv. Congr. Expo.*, pp. 1590–1602, 2009.

[2] Z. Chen, "Characterization and Modeling of High-Switching-Speed Behavior of SiC Active Devices," 2009.

[3] S. H.-M. H. M. Jen, C. C. C. Enz, D. R. R. Pehlke, M. Schroter, and B. J. J. Sheu, "Accurate modeling and parameter extraction for MOS transistors valid up to 10 GHz," IEEE Trans. Electron Devices, vol. 46, no. 11, pp. 2217–2227, 1999.







Appendix A-C3

Yasser Nour, Arnold Knott, and Ivan H. H. Jørgensen, " Implementation of a Dual on Die 140 V Super-Junction Power Transistors" e-poster in International Workshop on Power Supply on Chip (PwrSoC), Madrid, Spain, 2016.

Implementation of a Dual on Die 140 V Super-Junction Power Transistors

Nour, Yasser; Knott, Arnold; Jørgensen, Ivan Harald Holger

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Implementation of a Dual on Die 140 V Super-Junction Power Transistors

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Department of Electrical Engineering, Technical University of Denmark

Abstract

Increasing the switching frequency for switch mode power supplies is one method to achieve smaller, lighter weight and hopefully cheaper power converters.

Silicon is not only the dominant material used to produce the switches but also it allows more circuitry to be easily integrated on the same die.

This work presents an application customized switches to be used in switch mode power supplies.

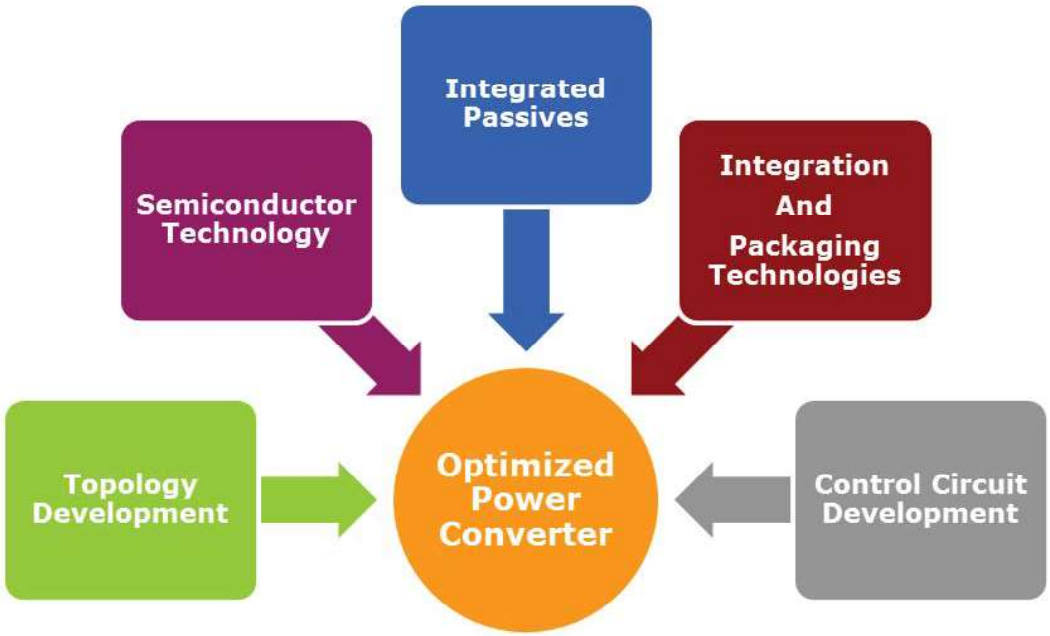
The prototype chip was implemented using a 0.18 µm SOI process and includes dual electrically isolated 140 V, 1.2 Ω N-channel MOSFETs.

Project Objectives

Wider Objective:
Develop an Integrated switch-mode power supplies utilize few external components.

Specific Objectives:
To integrate the DTU Elektro proven dc-dc converter topologies in a single module / chip.
To develop state of the art, high power density, high quality power supply prototypes.

Converter



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Implementation of a Dual on Die 140 V Super-Junction Power Transistors

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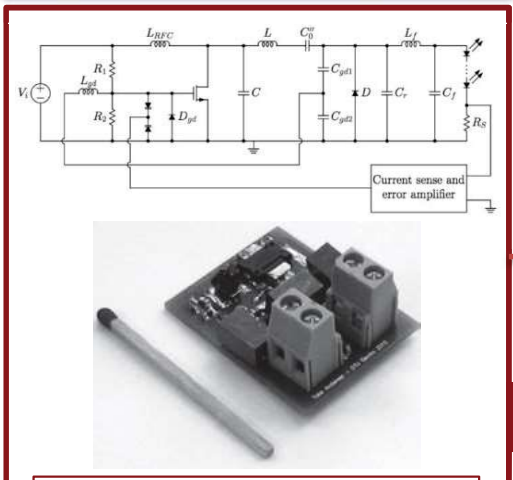
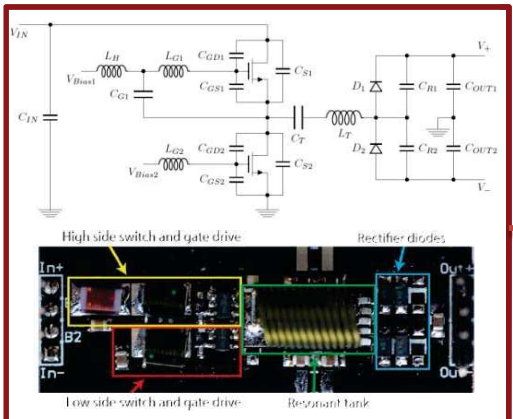
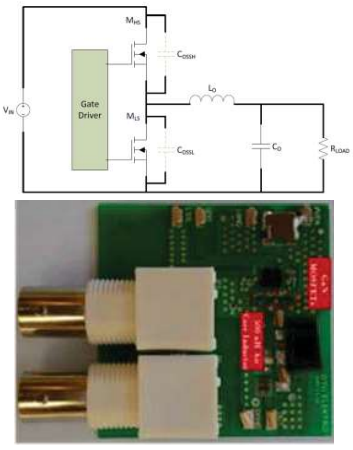
Single Cell Converters developed at DTU



Class E Resonant Converter *

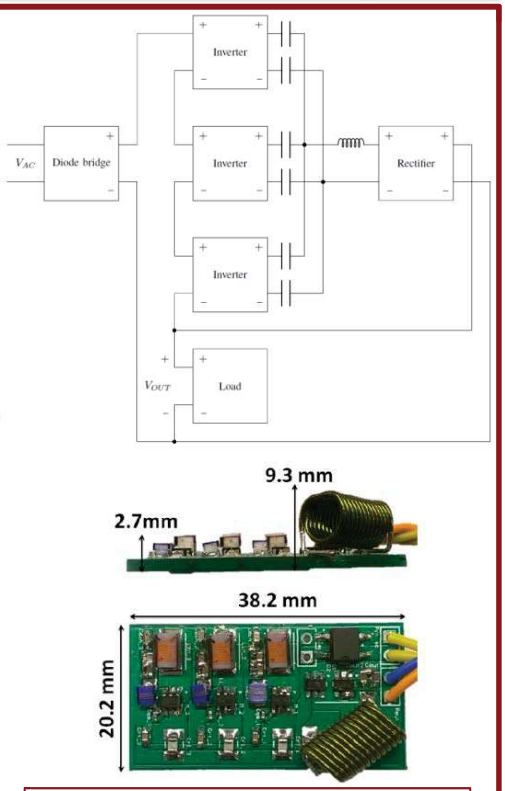


Class DE Resonant Converter **



Buck Converter ***

Stacked Cells Converter Developed at DTU



US Mains Converter****

* **Andersen, T.M. , Christensen, S.K. , Knott, A. , Andersen, M.A.E. , "**A VHF class E DC-DC converter with self-oscillating gate driver.", Applied Power Electronics Conference and Exposition (APEC), pages 885–891, March 2011

** **Madsen, M.P.; Knott, A.; Andersen, M.A.E.,** "Very high frequency half bridge DC/DC converter", Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE , vol., no., pp.1409-1414, 16-20 March 2014

*** **Yasser Nour, Arnold Knott, Ivan H. H. Jørgensen,** ; "Investigating Enhancement Mode Gallium Nitride Power FETs in High Voltage, High Frequency Soft Switching Converters," *IEEE International Conference on Power electronics, machines and drives (PEMD 2016)*, Glasgow, 2016.

**** **J. A. Pedersen, M. P. Madsen, J. D. Mønster, T. Andersen, A. Knott and M. A. E. Andersen,** "US mains stacked Very High Frequency self-oscillating resonant power converter with unified rectifier," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 1842-1846

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Implementation of a Dual on Die 140 V Super-Junction Power Transistors

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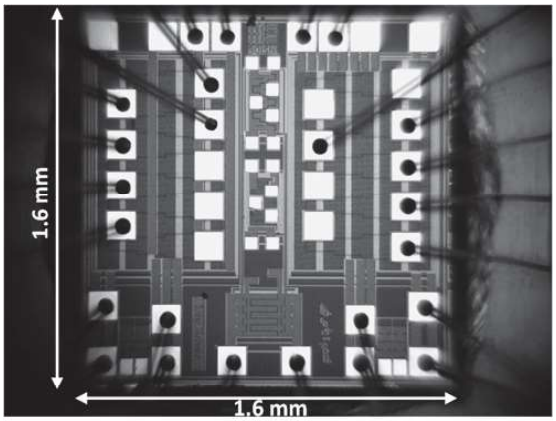
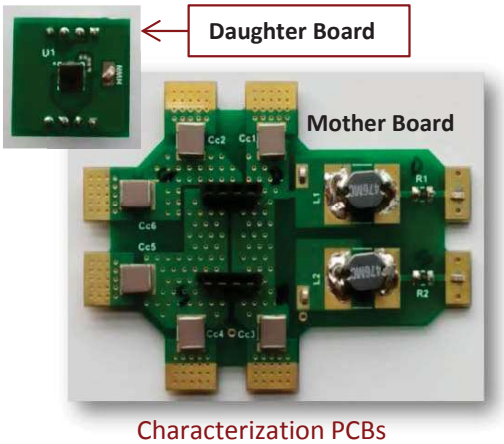
Semiconductor Technology

First Generation Switches

- Dual on Die" Electrically 140 V Isolated Super-Junction N-Channel Transistors.
- Using a 0.18 µm SOI process.
- Ron = 1.2 Ω for each switch. (@ 0.1 Vds)
- Designed for homogenous current distribution across the die.
- Die Size is 1.6 mm x 1.6 mm

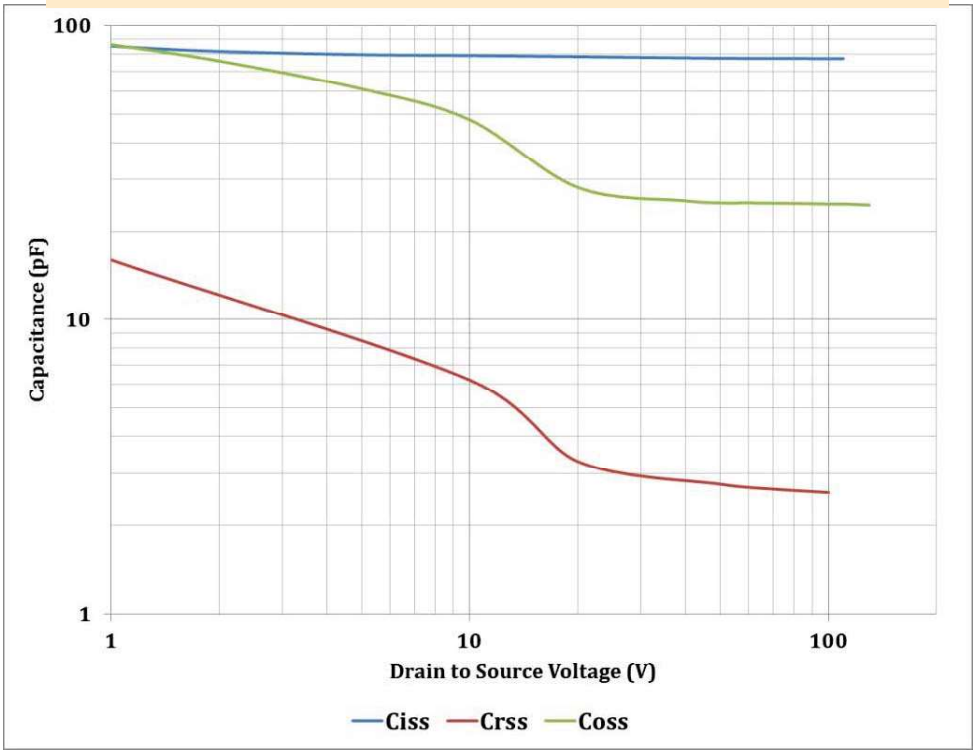


Photomicrograph of the designed chip



Characterization PCBs

Measured using Agilent 4294A precision impendence analyzer @ 1MHz



Characterization Results

Appendix A-C4

Yasser Nour, Ziwei Ouyang, Arnold Knott, Ivan H. H. Jørgensen, "Design and Implementation of High Frequency Buck Converter Using Multi-Layer PCB Inductor", The 42nd Annual Conference of the IEEE Industrial Electronics Society (IECON), Florence, Italy, 2016.

Design and Implementation of High Frequency Buck Converter Using Multi-Layer PCB Inductor

Nour, Yasser; Ouyang, Ziwei; Knott, Arnold; Jørgensen, Ivan Harald Holger

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Design and Implementation of High Frequency Buck Converter Using Multi-Layer PCB Inductor

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***Abstract*—Increasing the switching frequency for switch mode power supplies is one of methods to achieve smaller, lighter weight and cheaper power converters. This work investigates the opportunity of using two layer circular spiral inductors implemented in a 150 µm finished thickness printed circuit board for a high frequency DC-DC converter. The inductor was tested in a 5 W buck converter switching at 10 MHz. The converter achieved 84.7% peak efficiency converting 12 V to 5 V and 78% efficiency converting 24 V to 5 V.**

Keywords— PCB Inductors, Gallium Nitride, High Frequency Converters

I. INTRODUCTION

From the early beginning of using switch mode power supplies, it was obvious that the higher the switching frequency, the smaller the converters will be. Efficiency and thermal penalties were the limiting parameters for pushing the switching frequency to higher values. To develop such small power converters new semiconductor materials, innovative packaging, high frequency (300 KHz – 30 MHz) magnetics and development of converter topologies are the pillars for achieving efficient power conversion. It was clear that silicon switches have a lot of limitations when used in high switching frequency converters especially at elevated input voltages. Gallium nitride (GaN) based converters have shown a boost in converter efficiencies due to their lower parasitic capacitances and improved figure of merits [1, 2]

For the magnetic components, air core inductors are often being used in high frequency and very high frequency converters. Printed circuit board (PCB) planar air core inductors can be used as antenna or components for composing high-frequency matched filters in a Radio-frequency identification (RFID) system [3]. Recently, power supply on chip has gained their popularity and integrated air core inductors are often employed within very high frequency to achieve a higher power density [4-7]. PCB air core inductors do not need space to accommodate the magnetic core and have no core limitations such as core losses and saturation. Therefore, the size of PCB air core inductors can be significantly smaller, making it well suitable for applications that have stringent space and height requirements. The inductor windings manufactured by PCB machines are more precise and consistent, yielding the inductor designs with highly controllable and predictable parasitic parameters [8].

The frequency dependence of a PCB inductor must be considered under higher frequency. The eddy current effect at high frequencies dramatically increases effective resistance of a multi-turn spiral inductor winding. Current crowding is studied through approximate analytical modeling in [9].The non-uniform current distribution on the metallic trace is studied based on conventional magnetic flux method and energy method in [10]. Hurley et al. [11], presents a precise impedance formula with consideration of non-uniform current distribution and lossy magnetic media. Electromagnetic interference (EMI) is of particular concern in the PCB air core inductor working under multi-megahertz power converters. Unwanted stray magnetic fields can readily couple to near-by structures. It is well known that the addition of magnetics core plates to either side of the PCB winding provides enhancement of inductance values, and reduction of EMI problem. This paper focuses on the design and testing of a printed circuit board based inductor suitable for high switching frequency applications.

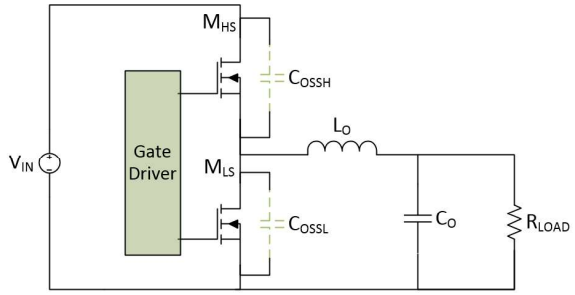
II. CONVERTER DESIGN

To test the inductors, a soft switching buck converter was chosen as it is the most basic step down switching converter. Zero-Voltage-Switching Quasi-Square-Wave (ZVS-QSW) was used as a switching technique. This switching technique uses the inductor current to charge or discharge the output capacitance of a semiconductor switches; resulting in much lower output capacitance related switching losses with a slightly higher conduction loss [1, 12, 13].Compared to hard switching buck converter, the total losses should be maintained lower by proper design. The detailed operation of ZVS-QSW buck converter was reported in [1]. Simple ZVS- QSW buck converter and the loaded converter's ideal waveforms are shown in Figure.1. The inductor value needed for a ZVS- QSW buck has to be less than the inductor value needed to operate a buck converter in critical conduction mode which is given by Equation.1 [14].

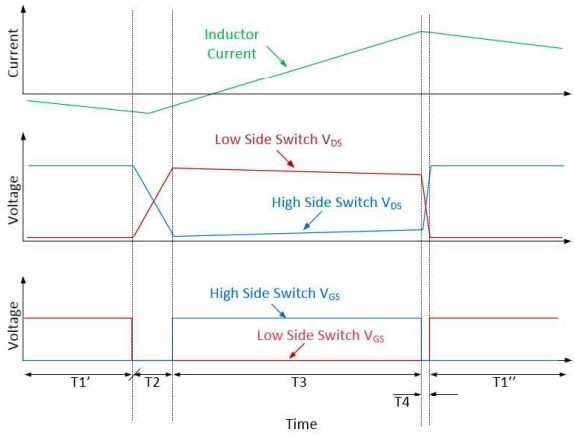
$$L_{O(min)} = \frac{(1-D)}{2F_{SW}} R_{Load} \quad (1)$$

For QSW-ZVS operation, it is important to assure the inductor current has the needed negative valley value based on equation.2 [14].

$$I_{Lo\,(min)} = I_{Load} - \frac{\Delta I_{Lo}}{2} = \frac{V_O}{R_{Load}} - \frac{V_O}{2L_O F_{SW}}(1-D) \qquad (2)$$



a. Power stage schematic.



b. Converter waveforms with load.

Fig. 1. Simplified QSW-ZVS Buck Converter [1]

Accurate gate drive timing is needed to achieve zero voltage switching and also to reduce the power loss in body diodes or power loss due to reverse conduction charge [14, 15]. The converter specifications are summarized in table 1. The critical inductance value needed is summarized in figure 2. To simplify the test procedure, the switching frequency was kept constant. This means the converter will be operating in hard switching during heavy load values and low input voltages.

TABLE.1 TEST CONVERTER SPECIFICATIONS

Parameter	Value	Description
V_{IN}	24 V	Input Voltage
V_{OUT}	5 V	Output Voltage
I_{OUT} (Max)	1 A	Maximum Output Current
F_{SW}	10 MHz	Switching Frequency

Switching at such high frequencies, it is required to choose high speed switches with low gate losses. The output capacitance related losses are minimized by the soft switching. A study was made in [1] comparing the figure of merits (FOMs) for both GaN FETs and silicon MOSFETs at different ratings of drain to source voltage. The results of that study are shown in figure 3 and figure 4 which clearly show the superiority of GaN FETs at all voltage levels. Two EPC8010 eGaN devices were chosen to carry out the design of the test converter for the inductors [16].

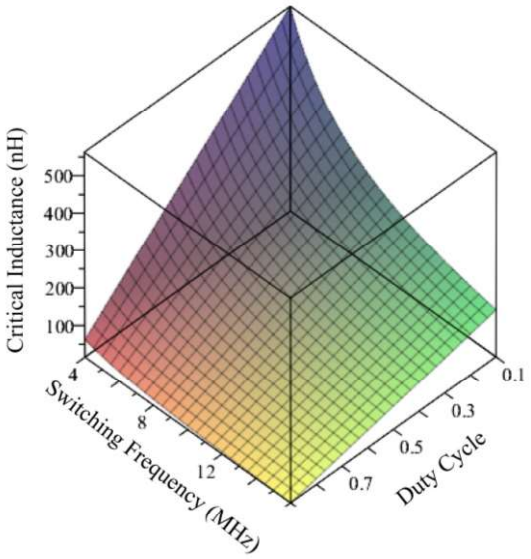


Fig. 2. Ideal critical inductance as a function of the switching frequency and duty cycle at 5V output voltage and 1A output current.

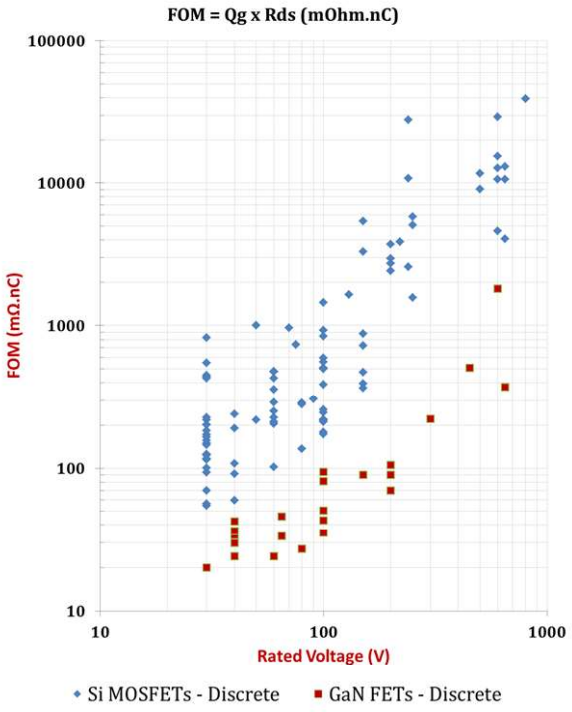
III. MODELLING AND FEA SIMULATIONS OF PCB INDUCTOR

For N_p turns spiral primary winding, the total self-inductance of the primary winding is the summation of each mutual inductance pairs between two concentric winding tracks, M_{ij}, where both i and j are from 1 to N_p. The self-inductance of the primary winding is given by Equation 3.

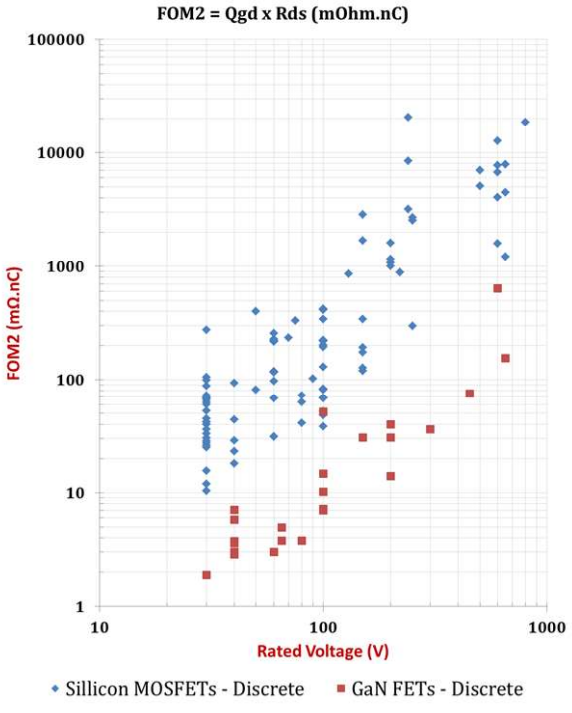
$$L_p = \sum_{j=1}^{N_p}\sum_{i=1}^{N_p} M_{ij} \qquad (3)$$

Figure 4 shows a generic cross-section of a PCB coreless inductor along 2-D X-Z plane. In practice a spiral arrangement would connect two layer sections in series, which can be accurately modelled by the concentric circular coils. Derivation of the mutual inductance, M_{ij}, in a PCB coreless inductor was proposed by Hurly [11, 17] and is given by equation 4.

The formulas have been derived from Maxwell's equations and therefore they can be fully expected to represent practical planar devices accurately. The extension of the formula can also cover the cases that the addition of magnetics core plates to either side of PCB winding structures.



a. Summary of high voltage FETs Q_{gtot}. R_{ON}



b. Summary of high voltage FETs Q_{gd}. R_{ON}

Fig. 3. Summary of gallium nitride vs. silicon FETs figure of merits [1]

$$M_{ij} = \frac{\mu_0 \cdot \pi}{h_1 \cdot h_2 \cdot In\left(\frac{r_2}{r_1}\right) \cdot In\left(\frac{a_2}{a_1}\right)} \cdot \int_0^{\infty} S(kr_2, kr_1) \cdot S(ka_2, ka_1) \cdot e^{-k \cdot z} \cdot Q(kh_1, kh_2) \cdot dk \quad (4)$$

where

$$S(kr_2, kr_1) = \frac{J_0(kr_2) - J_0(kr_1)}{k};$$

$$S(ka_2, ka_1) = \frac{J_0(ka_2) - J_0(ka_1)}{k};$$

$$Q(kh_1, kh_2) = \begin{cases} \frac{2}{k^2}\left(\cosh\ k \cdot \frac{h_1 + h_2}{2} - \cosh\ k \cdot \frac{h_1 - h_2}{2}\right), when\ z > \frac{h_1 + h_2}{2} \\ \frac{2}{k} \cdot \left(h - \frac{e^{-kh} - 1}{k}\right), when\ z = 0, h_1 - h_2 = h \end{cases}$$

μ0 *is permeability of airgap;*

h1 *is the height of the ith circular track;*

h2 *is the height of the j^{th} circular track;*

r1, r2 *are the inner and outer radius of j^{th} circular track;*

a1, a2 *are the inner and outer radius of i^{th} circular track;*

J0(x) *is first kind Bessel function of order zero;*

The model then was imported to Ansys Maxwell software for simulation and series resistance extraction. Figure 5 shows different views of the designed inductor and the design parameters are shown in table 2.

TABLE. 2. DESIGNED INDUCTOR PARAMETERS

Parameter	Value
h1 & h2	35μm
z	80μm
Track width	1mm
Track clearance	300μm
Inner coil radius	1.5mm
PCB size	12mm x 12mm

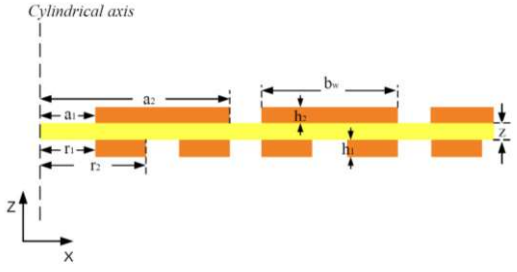


Fig. 4. A generic cross-section of a PCB inductor

Figure 6 shows FEA simulation of the current density (J) at 10 MHz using Ansys Maxwell. It is obvious from the figure that the current is pushed to the vertical edges of the spiral which impacts the AC resistance of the inductor.

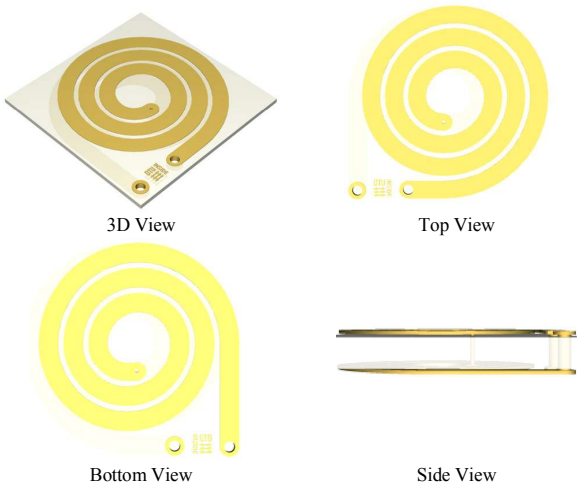


Fig.5. Two layer Ring Spiral Inductor

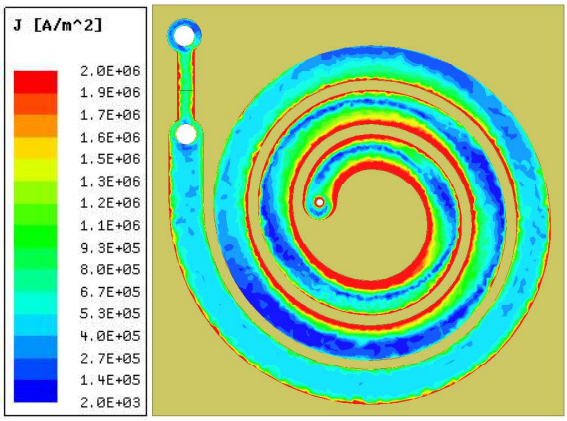


Fig.6. The current density at 10 MHz (top view)

IV. Experimental Results

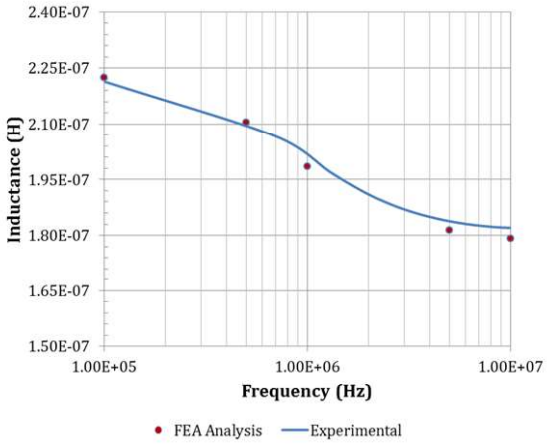
The two layer inductor prototype was manufactured and measured using an Agilent 4294A precision impedance analyzer. The results then compared to Ansys Maxwell FEA simulation results from 100 KHz to 10 MHz. A summary of series inductance and equivalent series resistance is shown in figure 7. The results show good matching between the simulation results and measurements.

The inductor was connected to the test buck converter. The measured efficiency versus output current of the converter at three different input voltages and a fixed output voltage is shown in figure 8. The converter has maximum efficiency of 84.7% at 12 V input voltage and 78% at 24 V input voltage. The total converter power loss is also shown in figure 9.

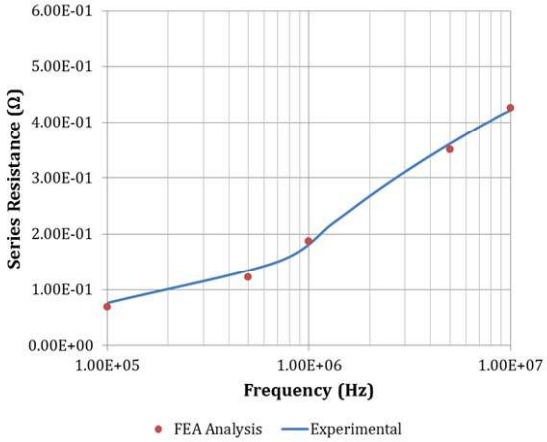
Based on the inductor characterization, the AC resistance at 10 MHz is 426 mΩ. Combining the DC and AC losses of the inductor, the total loss of the inductor is calculated and plotted versus the load current in figure 10.

V. Conclusion

In this paper, a two layer printed circuit board circular spiral inductor was experimented for a 5 W buck converter. Finite elements analysis for the inductor was carried out and the simulation results show good match to the measured inductance and the equivalent series resistance. The inductor was tested successfully in a buck converter circuit. The converter achieved 84.7% peak efficiency running at 10 MHz. the power stage was designed using gallium nitride power FETs and the gate driver signals were supplied from a dead time adjustment circuit.



a. Inductance vs. Frequency



b. Series resistance vs. Frequency

Fig.7. Ring spiral inductor FEA simulation results and Lab measurements

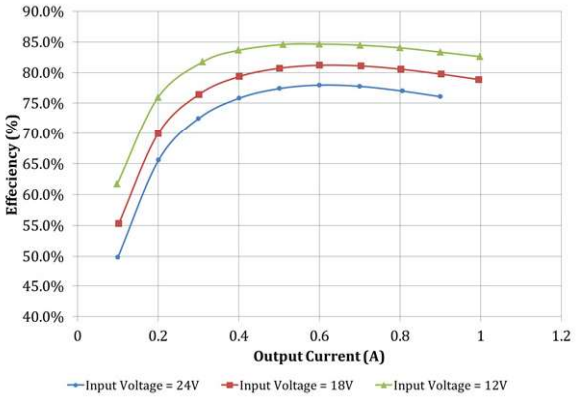


Fig.8. Efficiency vs. Output Current of the test converter at 5 V output voltage

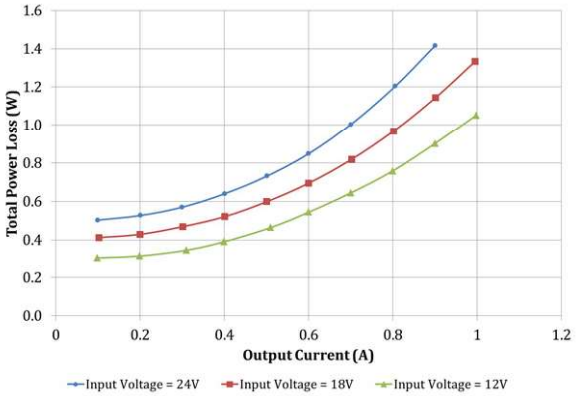


Fig.9. Total Power Loss vs. Output Current of the test converter at 5 V output voltage

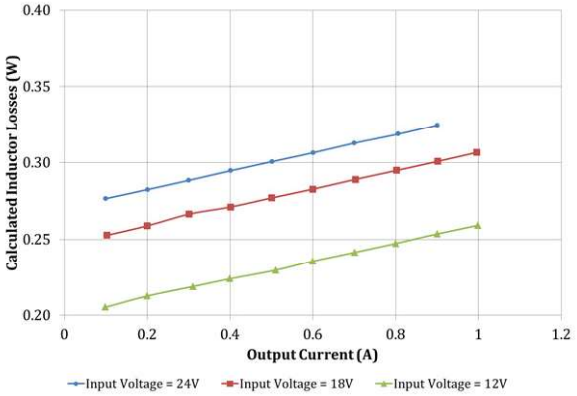


Fig.10. Total Inductor Power Loss vs. Output Current of the test converter at 5 V output voltage

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Appendix A-C5

Yasser Nour, Arnold Knott, Lars Press Petersen, "High frequency Soft Switching Half Bridge Series-Resonant DC-DC Converter Utilizing Gallium Nitride FETs", in the 19th European Conference on Power Electronics and Applications, (EPE), Warsaw, Poland, 2017.

High frequency Soft Switching Half Bridge Series-Resonant DC-DC Converter Utilizing Gallium Nitride FETs

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High frequency Soft Switching Half Bridge Series-Resonant DC-DC Converter Utilizing Gallium Nitride FETs

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Keywords

Gallium Nitride FETs, High-Frequency Converters, Soft-Switching, Class-DE Inverter

Abstract

The need for efficient, smaller, lighter and cheaper power supply units drive the investigation of using high switching frequency soft switching resonant converters. This work presents an 88% efficient 48V nominal input converter switching at 6 MHz and output power of 21 Watts achieving power density of 7 W/cm^3 for Power-over-Ethernet LED lighting applications. The switching frequency is used to control the output current delivered to the load resistance. The converter was tested using a constant resistance load. The performance and thermal behavior were investigated and reported in this work.

Introduction

Using high switching frequency (3 – 30 MHz) is one method to achieve smaller and lighter power converters [1, 2, 3]. To achieve efficient operation of the switches, soft switching techniques need to be used specially with elevated input voltages. Resonant converters allow the utilization of soft switching techniques due to the intrinsic alternating behavior of current and voltage through the switches. Soft switching is needed not only to achieve high efficiency but it also reduces electromagnetic interference (EMI) levels [4]. For LED lighting applications, a resonant converter serves the need for a constant current source. The resonant circuit can be designed to supply a constant current at the selected switching frequency. The switching frequency then can be used as a control parameter for the output current.

Resonant converters are relaying on exciting a resonant network to achieve power processing. Resonant DC-DC converters fundamentally consist of three stages. The first stage is to convert the DC input to an AC output. The second stage is the resonant circuit which can be modeled as an AC to AC converter stage. Combining the first and the second stages, results in an inverter circuit which converters a DC input to a desired level AC output. The third stage is the rectifier stage where energy is tapped off the resonant network to feed the output load [5]. A block diagram of the basic resonant DC-DC converter is shown in figure 1.

The basic inverter topologies are class E and class D. In class E based inverter, the voltage stress across the switches can be 3.5 to 4 times higher than the input supply voltage which will force to use devices with much higher breakdown voltages [6, 7, 8, 9, 10]. Class D inverter utilizes two switches with voltage stress equal to the input voltage which allows using higher speed, lower voltage devices

[9, 11]. Using two switches requires precise design of the gate driver circuitry to avoid cross conduction trough the two switches which may cause catastrophic failure of the converter. Many other inverter topologies also can be used but they involve extra circuit components to solve the problem of high voltage stress on the switches [9, 12].

This paper utilizes a soft switching half bridge series resonant converter to realize a high frequency DC-DC converter using gallium nitride (GaN) switches. The rectifier circuit also needs to be designed to be in the soft switching operation mode to avoid excess power losses and keeping the high efficiency of the entire system. A Power-over-Ethernet (PoE) powered device (PD) can be designed to have an input voltage between 37 to 57 VDC to support both PoE (IEEE 802.3af) and PoE+ (IEEE 802.3at). The PD can draw power up to 25.5 W according to the IEEE802.at standard or 12.95 W according to IEEE802af [13]. The proposed converter is intended to be used for PoE LED lighting applications. The output power delivered to the LED string can be controlled via the switching frequency. The converter specifications are summarized in table 1.

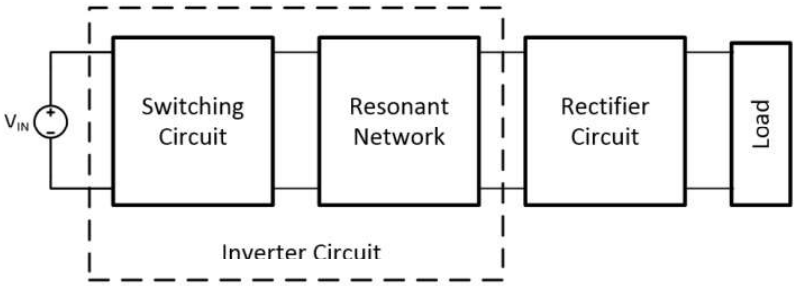


Fig. 1: Basic block diagram of a resonant converter

Table 1 : Converter Specifications

Parameter	Symbol	Value	Unit
Input Voltage Range	V_{IN}	37-57	V
Max. Output Power	P_{OUT_MAX}	21	W
Power Density		≥ 4	W/cm^3
Max. Output Voltage	V_{OUT_MAX}	30	V

Power Stage Design

A soft switching half bridge series resonant converter is shown in figure 2. Following the design steps in [4], the ideal design surface can be calculated using the following steps. The input resistance of an ideal half wave rectifier can be calculated using equation 1 according to [4]

$$R_{in\_rec} = \frac{2 \cdot R_{load}}{\pi^2} \tag{1}$$

Where R_{load} is the load resistance (50 Ω) – used as a test load.
Then the inverter's loaded quality factor can be calculated using equation 2 [4]

$$Q_L = \frac{\sqrt{\left(\frac{L}{C}\right)}}{R_{in\_rec}} \tag{2}$$

Where L is the inductance of the resonant tank, C is the capacitance of the resonant tank, and R_{in_rec} is the input resistance of the rectifier

The total voltage conversion ratio for the converter can be calculated using equation 3 [4]

$$M_V = \frac{1}{\sqrt{1 + Q_L^{\,2} \cdot \left(\omega_n - \frac{1}{\omega_n}\right)^2}} \tag{3}$$

Where ω_n is the normalized switching frequency and Q_L is the inverter loaded quality factor

The total voltage conversion ratio or voltage gain is plotted versus the loaded quality factor and the normalized frequency in figure 3. The rectifier is a half wave rectifier implemented using low forward voltage schottky diodes connected to the load resistance. Gallium nitride FETs show superior performance compared to silicon counterparts. A comparison based on datasheet parameters was reported in [14, 15] and shown in figure 4. The inverter is designed using EPC8010 gallium nitride FETs [16] from EPC driven by an LM5113 [17] half bridge gate driver from Texas Instruments, a 4.7 nF ceramic capacitor and a 491 nH AT536RATR49_SZ [18] air-core inductor from Coilcraft. The load resistance is set to 50 Ohms as a first order approximation to the LED string.
Based on the analysis and calculations, the converter is simulated using LTspice IV. Simulation results for the converter switching at 7 MHz and delivering around 15 Watts to the load are shown in figure 5. The output voltage is shown in the third subplot and it is 27.1 V.

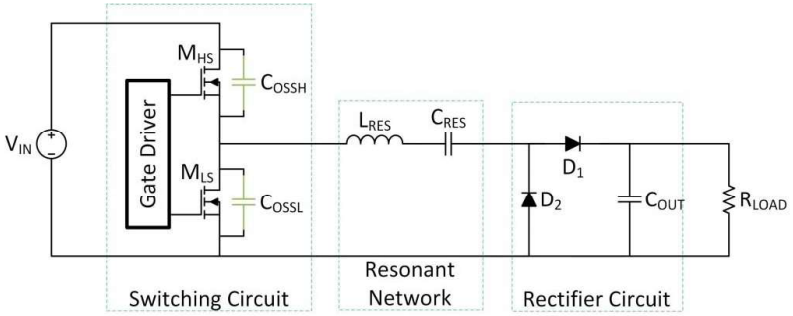


Fig. 2: Half Bridge series resonant converter

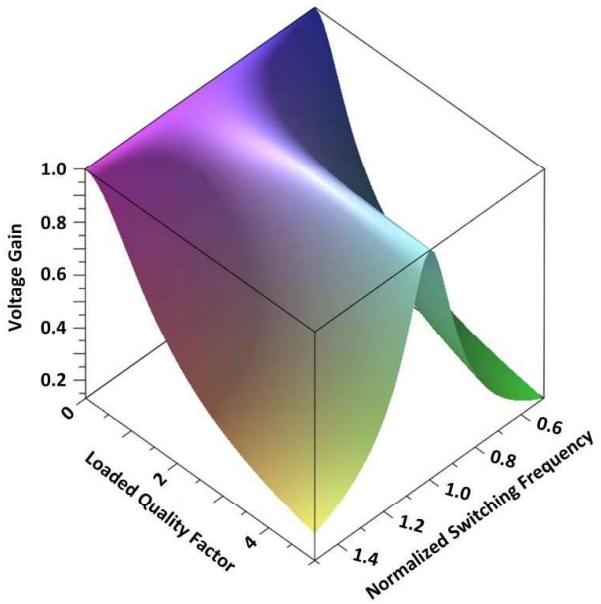
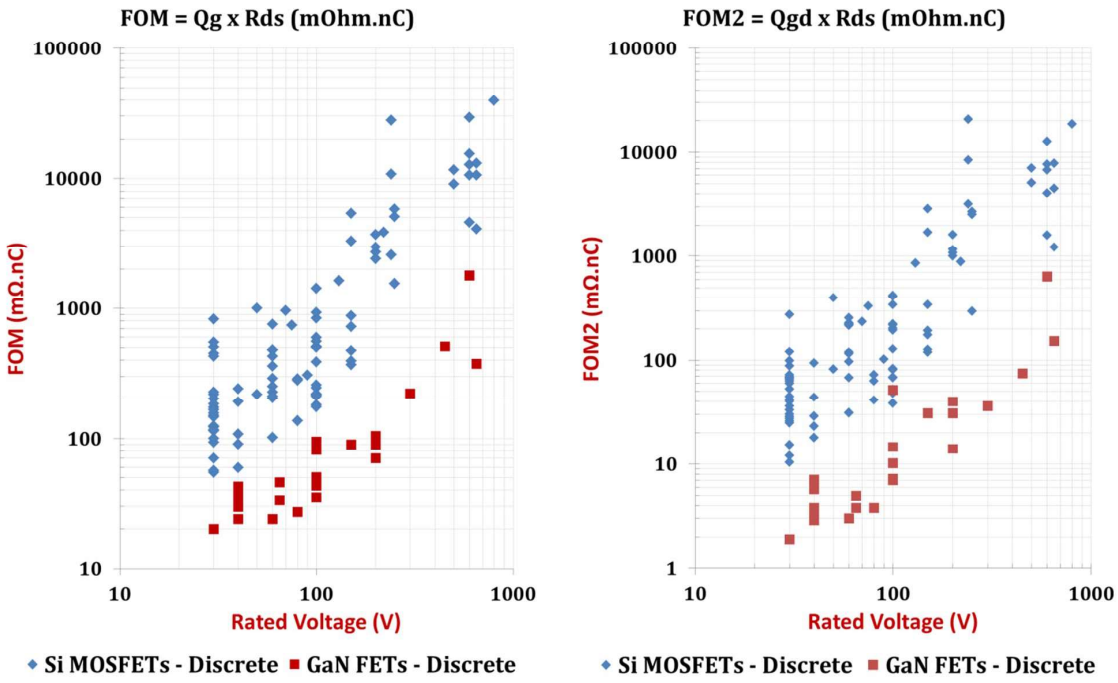


Fig. 3: Voltage Gain vs. Loaded Quality Factor and Normalized Switching frequency



a. Summary of high voltage FETs $Q_{gtot}.R_{ON}$ b. Summary of high voltage FETs $Q_{gd}.R_{ON}$

Fig. 4: Summary of gallium nitride vs. silicon FETs figure of merits [15]

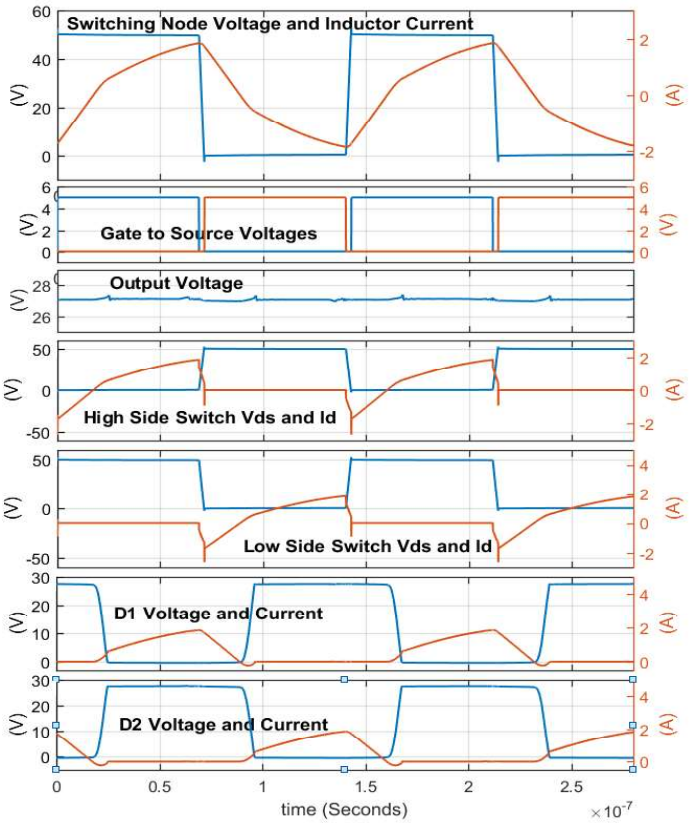


Fig. 5: LTspice IV simulation waveforms

Experimental Results

The converter is implemented and assembled on a two layer printed circuit board. The converter can operate at switching frequencies between 5 MHz and 8 MHz. The converter operation was continuously monitored using a thermal camera to fine tune the dead-time between the switches to achieve soft switching operation. To do so, the dead-time was manually fixed at a point where the average temperature of GaN FETs is minimized. Figure 6 shows a photograph of the prototype power stage.

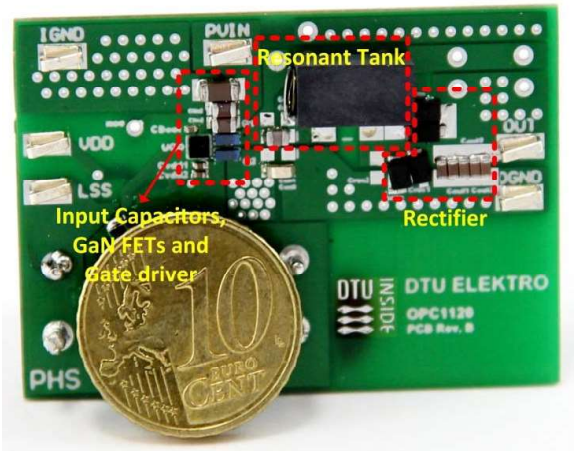
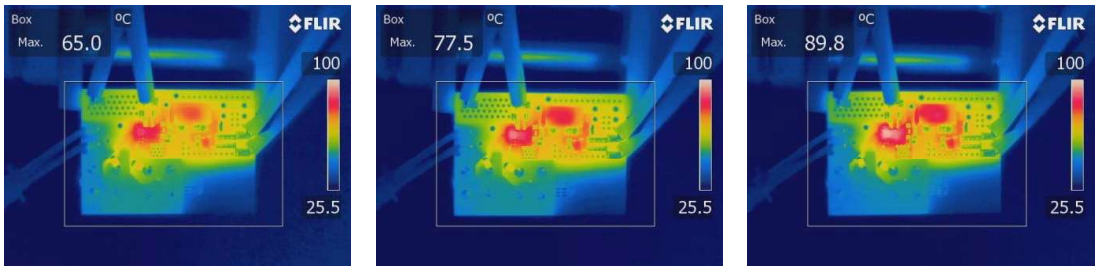


Figure 6: A Photograph of the test printed circuit board

The converter was tested for input voltages between 37 V and 57 V. Thermal photographs for three different input voltages for the converter switching at 6 MHz are shown in figure 7. The images show a maximum temperature of 89.8 C. The gate driver was detected to be the hottest element in the circuit.



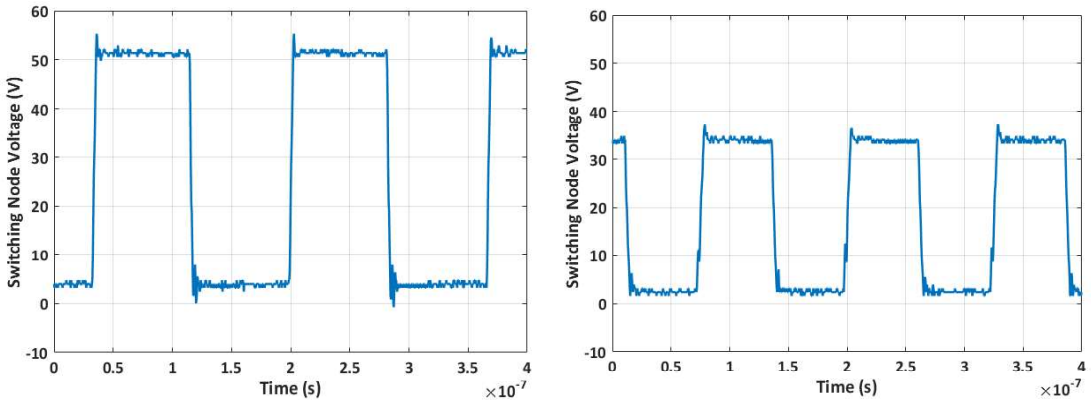
(a) V_{IN} = 37 V, F_{SW}= 6 MHz (b) V_{IN} = 48 V, F_{SW}= 6 MHz (c) V_{IN} = 57 V, F_{SW}= 6 MHz

Figure 7: Thermal images for the converter prototype

Due to the probe capacitance, measuring the switching node voltage while the converter is operating is shifting the operating condition. For sake of checking the switching performance, two sample waveforms were captured at two different frequencies. Figure 8a shows the switching node voltage when the input voltage of the converter is set to 57 V and switching frequency of 6 MHz. Figure 8b is the switching node voltage when input voltage is set to 37 V and switching frequency of 8 MHz. The switching node voltage waveforms were measured using a 2 GHz bandwidth oscilloscope and 500 MHz, 10x voltage probe with 9 pF capacitance.

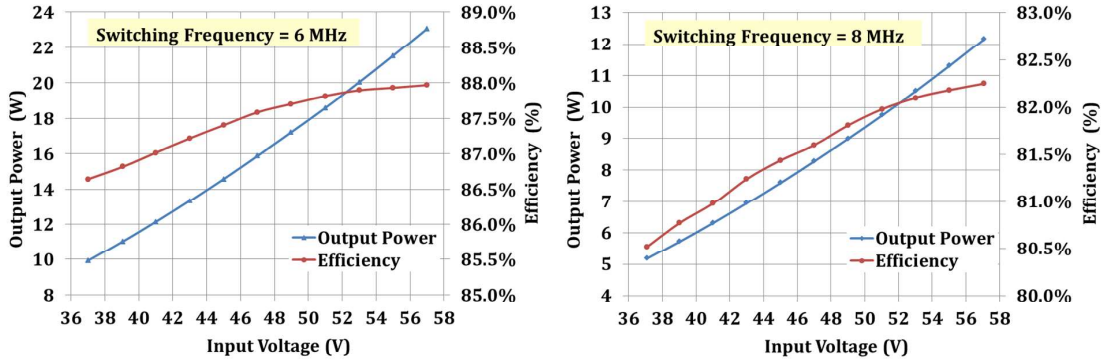
The converter's output power and efficiency versus input voltage are shown in figure 9 at two different switching frequencies. The peak efficiency of the converter switching at 6 MHz is 88% converting 57 V input voltage to 34 V output voltage and delivering 23 W to the 50 Ω resistive load. On the other hand, the peak efficiency at 8 MHz switching frequency was measured to be 82.2% converting 57 V

input voltage to 24.7 V and delivering 12 W to the load. Using the switching frequency as a control variable to choose the desired output current is investigated and the results are shown in figure 10. The figure shows the converter output current and efficiency versus switching frequency variation between 5 MHz and 8 MHz. the load was fixed to 50 Ω during all measurements.



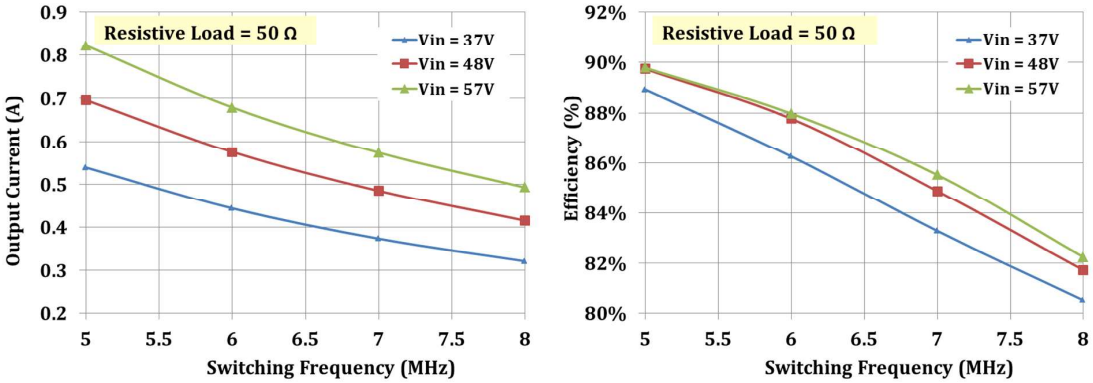
(a) V_{IN} = 57 V F_{SW} = 6 MHz (b) V_{IN} = 37 V F_{SW} = 8MHz

Figure 8: Switching node voltage measurements



(a) F_{SW} = 6 MHz (b) F_{SW} = 8 MHz

Figure 9: Measured output power and efficiency versus input voltage of the prototype



(a) Output current versus *Fsw* (b) Efficiency versus *Fsw*

Figure 10: Measured output current and efficiency versus switching frequency with 50 Ω load

Conclusions

In this study, gallium nitride FETs were tested to be used in a high switching frequency resonant DC-DC converter and they show promising results. Gate driver and dead time should be accurately fine-tuned on-the-fly not only to achieve high efficiencies but also to prevent hard switching from happening and causing a damage to the converter. The converter achieves 88 % efficiency when delivering a 21 W to the 50 Ohms load. The converter achieves a power density of 7 W/cm^3.

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Appendix A-C6

Hoà Thanh Le, Yasser Nour, Ziwei Ouyang, Arnold Knott, Flemming Jensen, Anpan Han, "3D MEMS Air-core Inductor in a Very High Frequency Switched-Mode Power Converter", in the 43rd International Conference on Micro and Nano Engineering (MNE), Portugal, 2017.

3D MEMS Air-core Inductor in a Very High Frequency Switched-Mode Power Converter

Lê Thanh, Hoà; Nour, Yasser; Ouyang, Ziwei; Knott, Arnold; Jensen, Flemming; Han, Anpan

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3D MEMS Air-core Inductor in a Very High Frequency Switched-Mode Power Converter

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Keywords: Inductors, power converters, zero voltage switching, gallium nitride FET, PwrSoC

Power supply on chip (PwrSoC) is the vision of miniaturized switched-mode power supplies with a monolithic integration of all active and passive components [1], [2]. Passive inductors are by far the most bulky and expensive parts in power supplies. Increasing operating frequency to very high frequency (VHF: 30 – 300 MHz) allows the usage of smaller inductors thus reducing the size of power supplies. Indeed, with the inductance of tens of nH [3], integrated air-core inductors are suitable for VHF power converters.

Last year we reported on the fabrication of a 3D MEMS air-core toroidal inductor. In the present work, we demonstrate its application in a power converter. The inductors are electrically characterized with small signal measurement, and tested in a VHF class E resonant boost converter.

Briefly, the MEMS inductor is designed with a silicon-embedded 3D construction consisting of through-Si vias (TSVs) arranged in a toroidal shape, suspended copper (Cu) windings, and Si fixtures [4]. The inductors are fabricated with a four-step 3D fabrication process (Fig. 1). These are (i) through-wafer deep reactive ion etching of TSVs, (ii) electroplating Cu TSVs and top and bottom Cu layers, (iii) spray coating of resist and wet etching, and (iv) removing Si core by isotropic ICP etching. The MEMS inductor is shown in Fig. 2a. The suspended windings are attached to the Si support die by five fixtures.

Air-core and Si-core inductors are electrically characterized and compared using an impedance analyzer (Agilent 4294a). The frequency is between 1 to 110 MHz. The tested inductors have 20 turns, 1.5 mm outer radius, 0.75 mm inner radius, and 350 µm height. The inductances are 44.6 nH and 43.9 nH for the air-core and Si-core inductor, respectively. Air-core inductors have superior performance with higher quality factor (Q) of 13.3 at 33 MHz compared to Q of 9 at 20 MHz of Si-core inductors. With the complete removal of the Si core, the parasitic capacitance reduces three folds from 11.5 pF to 3.7 pF, thus allowing a higher Q at higher frequencies. A higher Q indicates that air-core inductors have lower power losses than Si-core inductors, and therefore achieve a higher power conversion efficiency.

To demonstrate the application of our fabricated inductor, a VHF Class E resonant converter is designed, simulated with LT-SPICE, and implemented using our MEMS inductor (L_2) and a high-performance gallium nitride field-effect transistor as key components. The converter consists of a class E resonant inverter and a current-driven rectifier (Fig. 2b). The MEMS inductor is used as part of the resonant network in the inverter. It is glued onto the PCB by epoxy and the electrical connections are made by three gold wire bonds. The detailed working principle of the converter can be found in [5]. In brief, the converter is designed to operate at 33 MHz in zero voltage switching (ZVS) mode to reduce switching losses. The converter achieved an efficiency of 77% converting 8.4 V_{DC} to 12.4 V_{DC} and delivered 7.72 W to the load with a total loss of 2.32 W (Fig. 3). The simulated AC current in the MEMS inductor is 1 A RMS. The AC power loss in L_2 is estimated via DC power loss using thermal measurement method. An increasing DC current is driven through L_2 until the thermal images are match (Fig. 4). An AC power loss of 0.98 W is obtained.

At the MNE conference, we look forward to present in detail the applications of our air-core inductors in power supplies.

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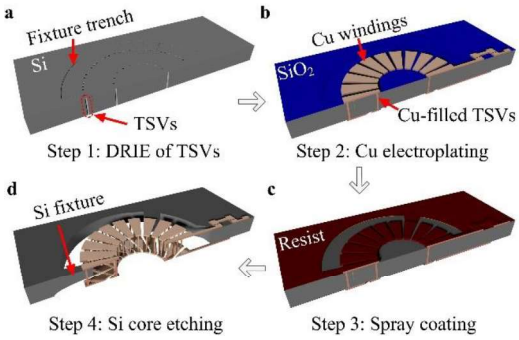

Figure 1 (a) Four-step fabrication process (direction A-A' in Fig. 2a).

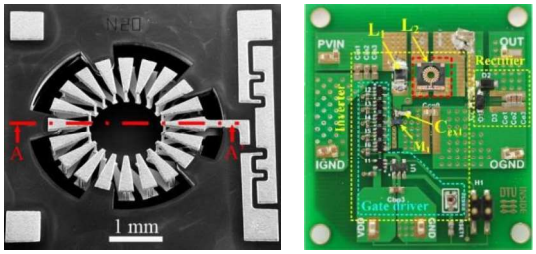

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Figure 2 (a) A SEM image of the fabricated MEMS air-core toroidal inductor. (b) Class E resonant boost converter with two parts: inverter and rectifier. The inductor (L_2) is connected to the PCB via gold bond wires.

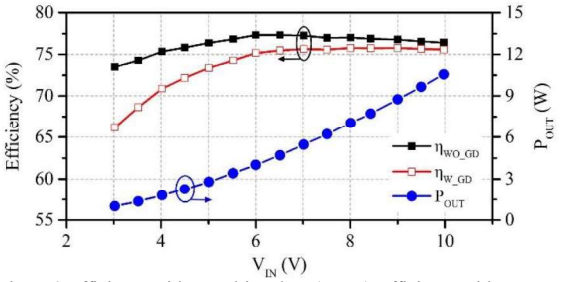

Figure 3 Efficiency with gate driver loss (η_{W_GD}), efficiency without gate driver loss (η_{WO_GD}), and output power (P_{OUT}) are measured with an input voltage sweep from 3 V_{DC} to 10 V_{DC}. The converter operates in zero voltage switching (ZVS) mode at 33 MHz and achieves an efficiency of 77% at V_{IN} = 8.4 V with an output power of 7.72 W.

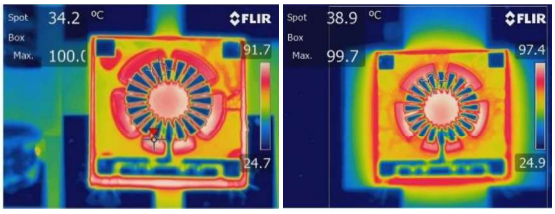

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Figure 4 Thermal performance of the fabricated air-core inductor in (a) an operating class E resonant boost converter which converts 8.4 V_{DC} to 12.4 V_{DC}, (b) a PCB test board with DC power loss. AC Power loss is estimated via DC power loss with temperature matching. The temperatures are matched at a 1.53 A DC current and 0.646 V DC voltage. AC power loss equals to DC power loss is 0.98 W

Appendix A-C7

Yasser Nour and Arnold Knott, "Module Integrated GaN Power Stage for High Switching Frequency Operation", in the 12th IEEE International Conference on Power Electronics and Drive Systems (PEDS), Hawaii, USA, 2017.

Module Integrated GaN Power Stage for High Switching Frequency Operation

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***Abstract*— an increased attention has been detected to develop smaller and lighter high voltage power converters in the range of 50 V to 400 V domains. The applications for these converters are mainly focused for Power over Ethernet (PoE), LED lighting and ac adapters. Design for high power density is one of the targets for next generation power converters. This paper presents an 80 V input capable multi-chip module integration of enhancement mode gallium nitride (GaN) field effect transistors (FETs) based power stage. The module design is presented and validated through experimental results. The power stage is integrated on a high glass transition temperature 0.4 mm thick FR4 substrate configured as a 70 pin ball grid array package. The power stage is tested up to switching frequency of 12 MHz. The power stage achieved 88.5 % peak efficiency when configured as a soft switching buck converter operating at 7 MHz. The converter is tested up to 12 W of output power at 13 V ± 1.5 V output voltage. The converter achieved a volume power density of 20 W/cm^3 and area power density of 9.4 W/cm^2.**

Keywords— Power Module, Gallium Nitride, High Frequency Converters

I. INTRODUCTION

Feature-rich electronic devices drive the demand for high power density dc-dc converters in order to minimize the application's printed circuit board area consumed by power supplies. Integration of power stages is one of the ways to achieve compact size, high efficiency and low noise power converters. Closer proximity of components or three dimensional packaging is needed to get the benefits from integrated power stages. The smaller the current loops are the more efficient and lower noise converters can be achieved [1, 2]. In addition, higher switching frequency operation can also be achieved due to the lower values of parasitic elements [1].

As shown in figure 1, an integrated buck converter typically requires power switches, magnetics, and capacitors, in addition to control and drivers for the power switches. The integration of such power stages can take different levels starting from multi-chip module (MCM) integration to power supply in package (PSiP) to power supply on chip (PSoC). Although PSoC has the potential to achieve the smallest solution size, it is very hard, if not impossible, to find a single fabrication process which covers high quality analog circuits, high switching frequency power switches, and passive components.

Manufacturing control and gate driver circuitry in silicon (Si) is the most cost effective way, not only due to the lower processing costs, but also the lower development costs of such circuits in silicon. On the other hand, wide bandgap materials (WBG) based power switches have been reported to have much smaller size and better switching performance than silicon switches especially for increasing voltages [3]. Gallium nitride (GaN) has a higher bandgap and electron mobility compared to silicon, silicon carbide (SiC) and gallium arsenide (GaAs), which make GaN the preferred semiconductor material for this research [3-6].

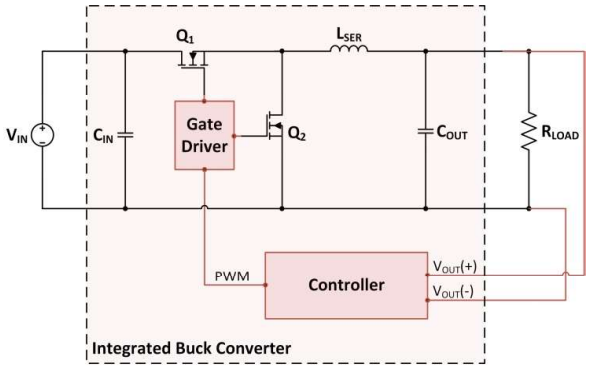


Figure 1: A typical integrated buck converter schematic.

This paper presents an 80 V input MCM integrated power stage utilizing quasi-square-wave zero-voltage-switching (QSW-ZVS) buck converter. The power stage operation theory, simulation, construction and experimental results are presented in this work.

II. CONVERTER THEORY OF OPERATION

Due to the excessive switching power losses in high frequency buck converter, it is required to use of a soft switching topology. One variant of a buck converter is the QSW-ZVS buck converter. In this switching technique, the inductor current has to be designed so that it has specific negative current amplitude. The inductor current to charges or discharges the output capacitance of a semiconductor switches; resulting in low output capacitance related switching losses with a slightly high conduction loss [4, 7, 8]. The total losses of a converter should be kept lower than conventional buck converter power stage by proper design. The inductor value needed for a ZVS- QSW buck has to be less than the inductor

value needed to operate a buck converter in critical conduction mode. The valley value of the inductor current depends on the summation of all the capacitances connected to the switching node. The detailed operation of ZVS-QSW buck converter was reported in [4, 9].

III. Power Stage Module Construction

The power stage is designed according to the specifications summarized in table 1 to operate at high frequency. The module integrates two 100 V rated eGaN FETs driven by a high frequency half bridge gate driver and an air-core inductor in addition to input and output capacitors. All the internal components are commercially available and summarized in table 2. Figure 2 shows the module schematic with all internal components. The module is built on a high glass transition temperature (High Tg) 0.4 mm thick FR4 substrate configured to form a 70 pin ball grid array (BGA) package. The finished size of the module is 9 mm x 12 mm x 4.7 mm. Pictures for the package are shown in figure 3.

The inductance value needed to implement this converter is much lower than it should be in a regular buck converter stage. The drawback of this topology is the high ac current flowing through the switches and inductor. Due to this fact, air-core inductor is used to eliminate the losses associated with using a magnetic core. Two variants of the module have been constructed to support wide range of input voltages and output power levels. The first variant uses a 390 nH ceramic core inductor supporting input voltage levels up to 60 V and output current up to 900 mA. The second variant uses a 1 uH ceramic core inductor supports input voltages of 60 V up to 95 V with output current capability of 700 mA.

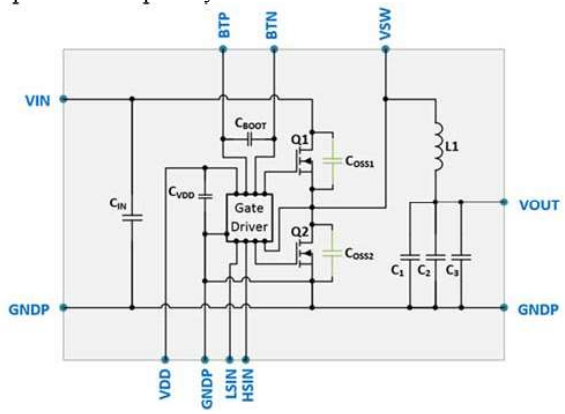
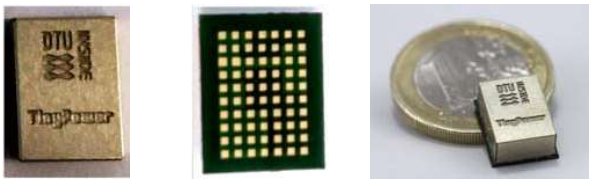


Figure 2: Schematic of the module.



Top side Bottom side On top of 1 Euro coin

Figure. 3: Photographs for the assembled module.

TABLE 1 TEST CONVERTER SPECIFICATIONS

Parameter	Value		Unit	Description
	Min.	Max.		
V_{IN}	--	95	V	Input voltage
V_{OUT}	--	24	V	Output voltage
D	12	80	%	Duty Cycle
F_{SW}	2	12	MHz	Switching Frequency
I_{OUT}	0	1000 *	mA	Variant 1 – V_{IN} < 60 V
	0	350	mA	Variant 2 – V_{IN} > 60 V

* maximum operating current depends on the input and out voltage to insure soft switching operation

TABLE 2 COMPONENT SELECTION

Comp.	Part No.	Qty.	Description
Q1 ,Q2	EPC8010	2	100 V GaN FETs [10]
L1	HA4036-AL	1	390 nH ceramic core inductor for input voltages lower than 60 V [11]
	1812CS-102XJL	1	1 uH ceramic core inductor for input voltages greater than 60 V [12]
C_{IN}	12061Z475KAT2A	1	Input capacitor [13]
C_1, C_2, C_3	C1005X5R1V225M050BC	3	Output capacitors [14]
U1	LM5113	1	High speed GaN FET gate driver [15]
C_{BOOT}	GRM155R71E473KA88D	1	Bootstap capacitor [16]
C_{VDD}	C1005X5R1V225M050BC	1	Decoupling capacitor of the gate drivers [14]

IV. Converter Simulations

A simulation model is constructed and simulated using LTSPICE software. Variant 1, with the 390 nH inductor, simulation results are shown in figure 4. The input voltage for this simulation is 40 V, the output voltage is 13 V, and output power of 12 W. The converter is switching at 7 MHz. The first subplot shows the switching node voltage and the inductor current. A 600 mA negative current can be observed from the simulations, and the stored energy is used to charge the capacitances connected the switching node, mainly the output capacitances of the GaN FETs. The second subplot shows the gate to source voltages of the two GaN FETs. As it can be observed, asymmetrical dead-time is introduced to achieve soft-switching operation and minimize the reverse conduction loss, which is similar to body diode conduction for silicon FETs.

The power stage simulated waveforms under no load condition are shown in figure 5. In this case, the introduced dead-time is symmetrical and short to avoid extra losses due to reverse conduction for the GaN FETs. It is possible to keep the dead-time fixed, optimized for heavy load condition, instead of implementing a variable dead-time controller. This will ensure soft switching operation at heavy loads but will result in lower efficiency at light loads. This concept is tested experimentally to evaluate if it will cause any failure.

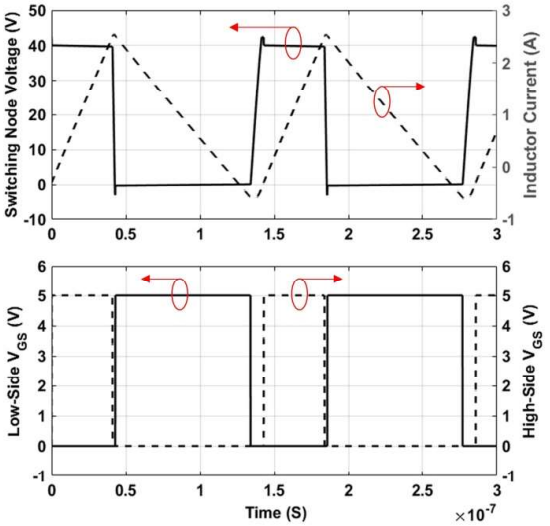


Figure 4: Simulated waveforms of power stage under loading condition and switching at 7 MHz switching frequency.

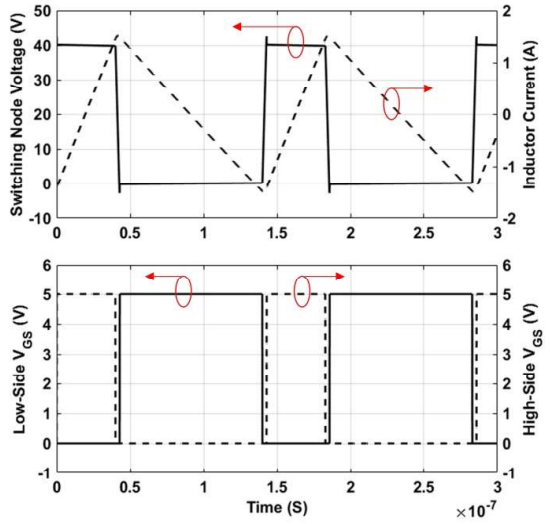


Figure 5: Simulated waveforms of power stage under no-load condition and switching at 7 MHz switching frequency.

V. Experimental Results

The power stage module is mounted on a test board to test the functionality of the converter. Input signals for the gate driver (LSIN and HSIN) are supplied via a function generator.

A photograph of the module mounted on the test board is shown in figure 6. The dead time is adjusted for achieving ZVS operation at heavy load conditions. To monitor the thermal behavior of the converter, an open lid module is tested in a soft-switching buck converter configuration. Figure 7 shows the basic switching waveforms of the converter with input voltage of 40 V, output voltage of 13 V, switching frequency of 7 MHz, and the load current is set to 900 mA using an electronic load. Figure 7(a) shows the switching node measured using a 500 MHz bandwidth 10X Rohde & Schwarz probe although the channel bandwidth is limited to 200 MHz. Figure 7(b) shows the low side gate voltage measured using an active probe to minimize the effect of probe loading on the measurements. The oscilloscope channel bandwidth is limited to 800 MHz.

Under the same testing conditions mentioned in the description of figure 7, the thermal photograph shown in figure 8 is captured after removing all the testing probes to eliminate the probe capacitance effects on the circuit operation. The thermal image shows a peak temperature of 81.4 ^{O}C on the surface of the inductor. The switches are showing 59 ^{O}C and the gate driver chip temperature is measured to be 65 ^{O}C.

The efficiency curve versus output power of the unregulated power stage is shown in figure 9.

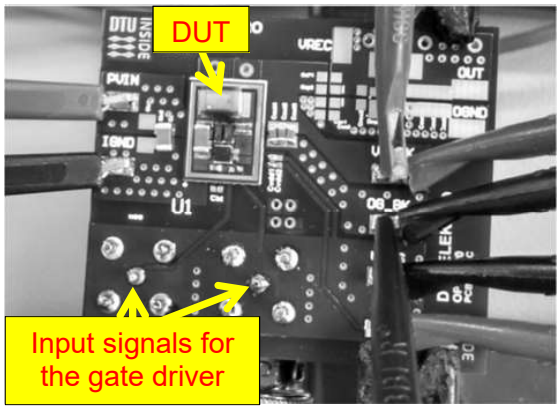


Figure 6: The open lid device-under-test (DUT) mounted on the test board.

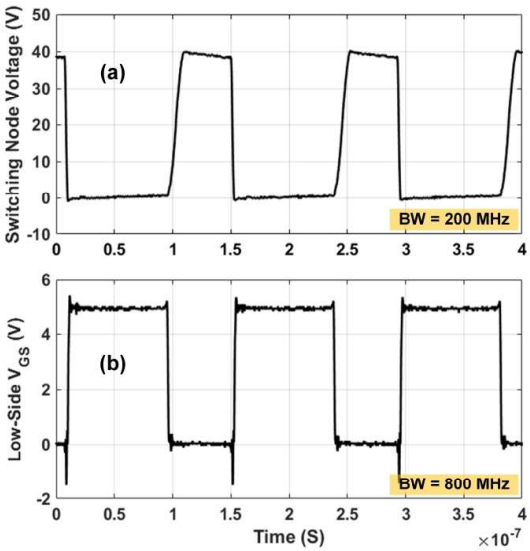


Figure 7: Measured waveforms of the loaded power stage input voltage of 40 V, output voltage of 13 V, the load current is 900 mA, and switching frequency of 7 MHz.

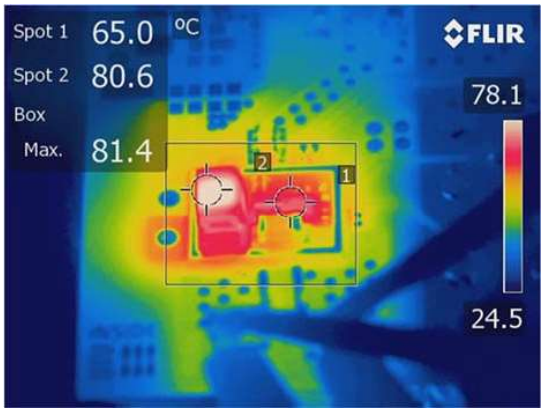


Figure 8: A thermal photograph of the module (variant 1) at 40 V input and 13.5 V output for 900 mA load.

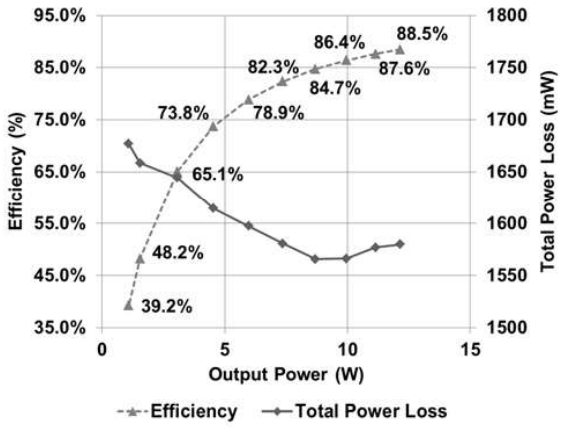


Figure 9: Efficiency and total power loss versus output power of the unregulated power stage at input voltage of 40 V, switching frequency of 7 MHz and fixed dead-time.

The second variant of the power stage is realized by exchanging the 390 nH inductor by a lower rated current ceramic core 1 µH inductor. The second variant is tested at two different input voltages.

The first test is performed at input voltage of 60 V and the switching frequency is set to be 8 MHz. The switching node voltage waveform is shown in figure 10, which shows a smooth transition to the rail voltage. The efficiency and total power loss curves are shown in figure 11. The peak efficiency is 84 % converting an input voltage of 60 V to an output voltage of 11.1 V at a load current of 700 mA.

The second test is performed at input voltage of 80 V and the switching frequency was set to 5 MHz. The switching node voltage waveform is shown in figure 12, which shows a smooth transition to the rail voltage. The converter's efficiency curve is shown in figure 13. The efficiency peaks at 76.2 % when converting an input voltage of 80 V to 13.5 V at 350 mA load current.

VI. Conclusion

Gallium nitride FETs based module on a printed circuit board is developed and experimentally tested up to input voltage of 80 V. The module achieved 88.5 % peak efficiency when tested as a 40 V input buck converter. The testing shows operation up to 12 MHz switching frequency at low input voltages. The dead-time can be adjusted using two methods. The first method is a fixed dead-time method, where the dead-time is adjusted at the heaviest load condition; the second method is a variable dead-time method, which requires fine tuning the dead-time with any change of the load, input voltage, output voltage or frequency. The variable dead-time method has potential to achieve higher efficiencies especially at light load conditions.

ACKNOWLEDGMENT

This work is conducted in the department of electrical engineering, Technical University of Denmark (DTU). This project is a part of TinyPower project which is funded by Innovation Fund (No. 67-2014-1).

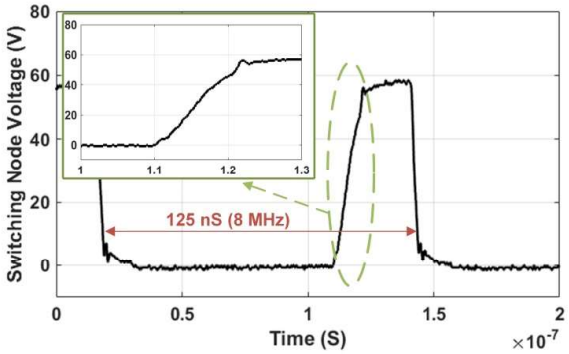


Figure 10: Switching node voltage at input voltage of 60 V, output voltage of 12 V, 650 mA load current and switching frequency of 8 MHz.

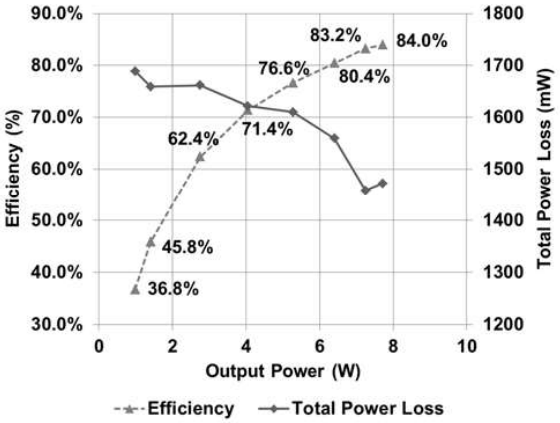


Figure 11: Efficiency and total power loss versus output power of the unregulated power stage at input voltage of 60 V, switching frequency of 8 MHz and fixed dead-time.

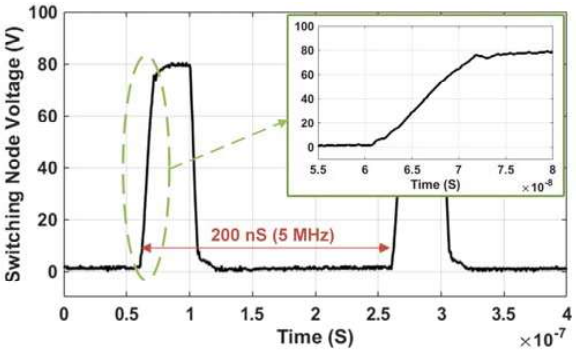


Figure 12: Switching node voltage at input voltage of 80 V, output voltage of 14.1 V, 200 mA load current and switching frequency of 5 MHz.

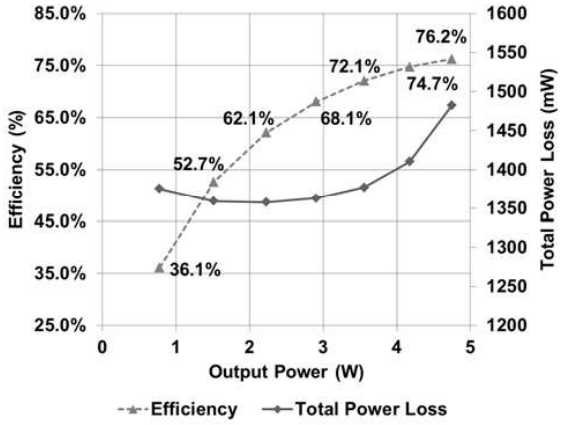


Figure 13: Efficiency and total power loss versus output power of the unregulated power stage at input voltage of 80 V, switching frequency of 5 MHz and fixed dead-time.

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Appendix A-C8

Christopher Have Kiaerskou Jensen, Frederik Monrad Spliid, Jens Christian Hertel, Yasser Nour, Tiberiu-Gabriel Zsurzsan, and Arnold Knott, "Resonant Full-Bridge Synchronous Rectifier Utilizing 15V GaN Transistors for Wireless Power Transfer Applications Following AirFuel Standard Operating at 6.78MHz", in the Applied Power Electronics Conference and Exposition (APEC), TX, USA, 2018

Resonant Full-Bridge Synchronous Rectifier Utilizing 15 V GaN Transistors for Wireless Power Transfer Applications Following AirFuel Standard Operating at 6.78 MHz

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***Abstract*—Connectivity in smart devices is increasingly realized by wireless connections. The remaining reason for using connectors at all is for charging the internal battery, for which wireless power transfer is an alternative. Two industry standards exist to support compatibility between devices. This work is focusing on the AirFuel standard, as it is operating at a higher frequency (6.78 MHz) and therefore allows smaller passive components, including the coupling coils. Whereas gallium-nitride (GaN) devices are being widely used on the transmitter (Tx) side, this work uses low voltage GaN transistors on the receiver (Rx) side to allow synchronous rectification and soft switching, thereby achieving high efficiency. After analyzing adequate Class-DE rectifier topologies, a Class-DE full-bridge 5 W rectifier using 15 V GaN transistors are designed and implemented. The experimental results show an efficiency above 80 % over a wide operating range and a peak efficiency of 89 %, at an arbitrary alignment of Tx and Rx coil with 3 cm distance between them.**

***Index Terms*—Wireless power transfer, AirFuel, synchronous rectification, resonant circuit, soft-switching, GaN devices.**

I. Introduction

In recent years, the attention to wireless charging technologies for consumer applications, as shown in Fig. I, has grown dramatically. Avoiding the connectors in smart phones and tablets allow for a further increase in their robustness (e.g. water proof cases) and gives more space for energy storage in the battery to increase the battery life. Therefore, two standards were created; Qi [1] and AirFuel [2]. Research activities, addressing the lower frequency (87 - 205 kHz) Qi standard [3], [4], [5], [6], [7] and the higher frequency (6.78 MHz) AirFuel standard [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18] grew as well. Some work [19], [20] are targeting both standards and other work [21], [22] reported operation outside those standards. As higher frequencies promise size reduction of passive components and in terms of wireless charging applications, especially smaller transmitter (Tx) and receiver (Rx) coils - this work focuses on the AirFuel standard. Gallium nitride (GaN) devices are used in [12], [15], [18] to reduce switching losses on the Tx side. Synchronous rectifiers, typically used in high power applications [23], [24], address the conduction losses on the Rx side in [3], [7], [13]. This work combines these two advantages on the Rx side with a synchronous rectifier based on GaN devices, fulfills the AirFuel standard [2] and addresses the specification in table I.

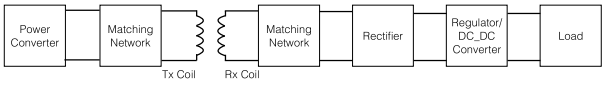


Fig. 1. Block diagram of the elements in a WPT system

TABLE I
Design specifications

Output power P_{out}	5 W
Output voltage V_{out}	5 V
Operating frequency f_{sw} [2]	6.78 MHz

II. Topology selection

Synchronous rectification for WPT is being researched, as it is a potential way to overcome the losses associated with diodes, which are currently used in WPT systems. Other work such as [4], [7], [3], [25], [26], [27], [13], [14] looks into ways of implement and optimize control schemes for synchronous rectifiers.

This work uses a comparator to sense the voltage across the synchronous rectifier, as shown in Fig. II. To overcome propagation delay of the gate driver, a delay is implemented between the comparator and the gate driver. This helps correct the delay of the last period in the next switching period, which is tuned to achieve soft switching.

Resonant topologies [10], [14], [16], [17], [28] are very promising for wireless charging applications, as they allow precise impedance matching to the Tx and Rx coils and simultaneously provide high energy efficiency due to their ability to soft-switch the power devices.

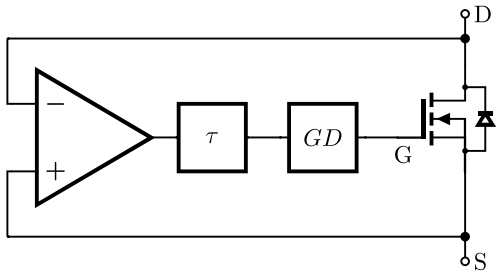


Fig. 2. Concept drawing of the synchronous rectification circuit

Whereas [10], [14], [16], [17], [28] use the Class-E topology to avoid high-side switches and therefore come with a high voltage stress across the power semiconductor, [29], [30] document the Class-DE topology and its corresponding high-side gate driver [31], [32] as alternative. Within the current-driven Class-DE rectifier family, Fig. 3 shows three members.

For the implementation in this work, each of the diodes is replaced with a comparator-transistor combination shown in Fig. II.

Three topologies where investigated. The Class-DE half-bridge rectifier described in Fig. 3a [33] , a Class-DE full-bridge rectifier based on the half-bridge Fig. 3b and the half-wave Class-DE low dv/dt rectifier described in Fig. 3c [34]. These three topologies were simulated in LTspice with synchronous rectification instead of diodes. To find the transistor with the best performance for the specifications, multiple transistors where analyzed using figures of merit (FOM).

A. Transistor FOM Analysis

With the help of figures of merit, see (1) - (3), several potential power devices are investigated based on their datasheet parameters [35], [36], [37], [38], [39], [40]. The result of the investigation can be seen in table II.

$$FOM_1 = Q_{ISS} \cdot R_{DSon} \tag{1}$$

$$FOM_2 = Q_{Gtot} \cdot R_{DSon} \tag{2}$$

$$FOM_3 = Q_{OSS} \cdot R_{DSon} \tag{3}$$

The FOM2 says somthing about the frequiency range the device can operate in, but the focus is on the input characteristics FOM1 and the output characteristics FOM3. Q_{ISS} and Q_{OSS} are the input charge and output charge of a transistor respectively. It is important to integrate the input and output capacitances C_{ISS} and C_{OSS} in the full drain-source voltage interval to get Q_{ISS} and Q_{OSS}, as these capacitances vary with voltage. R_{DSon} is the resistance from drain to source when the transistor is in the ON-state. This method of evaluating transistors based on their FOM has also been done in works like [41].

Comparing the GaN EPC2040 [35] device in table II with the silicon (Si) based devices [36], [37], [38], [40], the GaN device is superior by a factor of 3 with respect to FOM1 and FOM3 and therefore chosen. A visualization of the transistor FOM can be seen in Fig. 4.

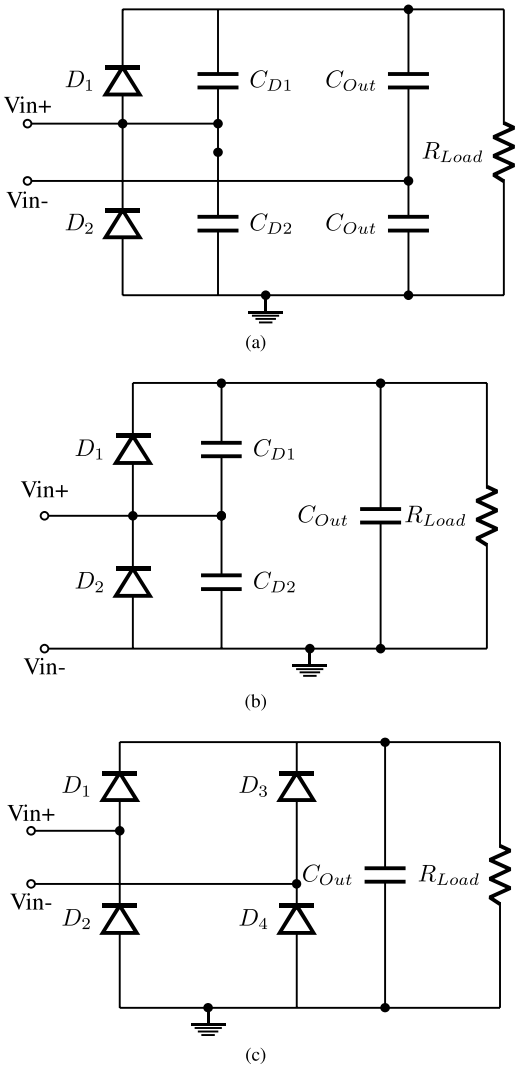


Fig. 3. Current driven soft-switching rectifier circuits

The method presented in [34] with the specifications from this work, results in the need of extra capacitance at the drain-source of each transistor. As the EPC2040 only has 70 pF drain-source capacitance [35]. The equations from [34] are shown in (4) and (5). Where I_{out} and I_m are the output current and magnitude of the input current respectively. V_{out} is the output voltage, C_{D1} and C_{D2} are the drain-source capacitance and ω is angular frequency of the input signal.

$$I_{out} = \frac{I_m}{2\pi} \rightarrow I_m = 6.28\,\mathrm{A} \tag{4}$$

$$V_{out} = \frac{I_m}{\omega(C_{D1} + C_{D2})} \rightarrow C_{D1} + C_{D2} = \frac{I_m}{V_{out} \cdot \omega} \rightarrow C_{D1} = C_{D2} = 14.75\,\mathrm{nF} \tag{5}$$

TABLE II
TRANSISTOR SELECTION BASED ON FOM1 AND FOM3 BASED ON DATA FROM [35], [36], [37], [38], [39], [40]

Transistors:	Voltage Rating [V]	R_{DSon} [$m\Omega$]	Q_{iss} [pC]	Q_{oss} [pC]	FOM_1 [pVs]	FOM_3 [pVs]
EPC2040 (GaN) [35]	15	28	523	357	14.64	9.996
SiUD412ED (Si) [37]	12	340	128	102	43.72	34.68
Si4838DY (Si) [38]	12	3	25197	15717	75.59	47.15
Si2342DS (Si) [39]	8	17	5711	2508	97.08	42.63
DMN1260UFA (Si) [40]	12	366	428	211	156.52	77.35
Si1050X (Si) [36]	8	86	3169	1277	272.59	109.83

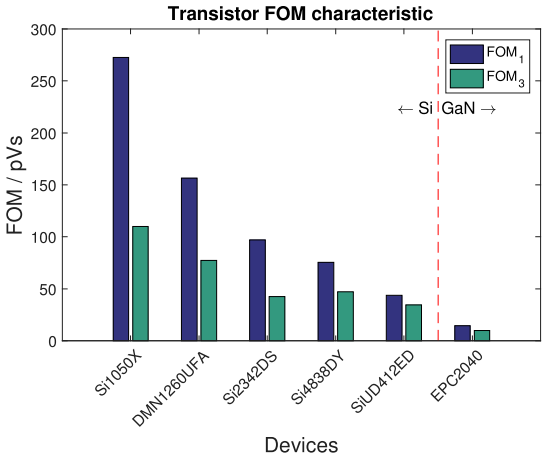


Fig. 4. Visualization of the transistors FOM values

Any deviation from soft-switching would result in large switching losses due to the added capacitance, which is undesired. With the added capacitance the input current amplitude is 6.28 A, see equation (4). In the simulation, it is found that having only the drain-source capacitance of the EPC2040 results in an input current amplitude of 3.14 A, for both half-bridges. The input current amplitude of the full-bridge is 1.57 A, when using only the EPC2040 drain-source capacitance.

B. Component Stress Factors

Component stress factors (CSF) are used to evaluate the three topologies and to see which best fit with the specifications. As there are no inductive elements in any of the three topologies only the semiconductor stress factor (SCSF) and capacitive component stress factor (CCSF) is calculated, see (6) and (7).

$$SCSF_i = \frac{\sum_j W_j}{W_i} \frac{V_{max,i}^2 I_{RMS,i}^2}{P^2} \tag{6}$$

$$CCSF_i = \frac{\sum_j W_j}{W_i} \frac{V_{max,i}^2 I_{RMS,i}^2}{P^2} \tag{7}$$

Here V_{Max} is the maximum voltage the component experience and the I_{RMS} is the RMS current running in that component. W_j and W_i are weighting factors. In this work, each stress factor is weighted equally. P is the output power of the converter.

The voltages and currents V_{Max} and I_{RMS} for each component in each converter are found via the LTspice simulation. The total SCFS ans CCSF for each converter are shown in table III.

TABLE III
CALCULATED COMPONENT STRESS FACTORS OF THE TOPOLOGIES WITHOUT WEIGHTING

Topology:	SCSF	CCSF
Class DE Half-Wave low dv/dt Rectifier:	4.93	1.47
Class DE Half-Bridge Rectifier:	4.93	0.74
Class DE Full-Bridge Rectifier:	2.47	0.25

It can be seen that the full-bridge experiences the fewest stresses on the components. Furthermore, it also has a small amplitude on the output voltage ripple due to the fact that it conducts power in both switch periods. This is also the reason for the lower input current. Based on the CSF The full-bridge topology is chosen.

III. IMPLEMENTATION

Choosing the GaN device EPC2040 [35] for synchronous rectification, a GaN compatible gate driver is required. The gate driver also have to have a supply voltage lower than the output voltage of the receiver, as it would in a commercial product be supplied from the output. In this work the drive circuitry is supplied from an external source to ensure performance stability in the tests. A block diagram of the full-bridge rectifier is shown in fig III, with the four EPC2040 GaNFETs and two LM5113 gate drivers. The voltage sensor and delay compensation for each high side controls the drive signals for the high side in one branch and the low side for the other branch. The delay compensation has been empirically tuned for these exact components. V_D is representing the external source for the control circuit. The gate resistors R_{Gate} limits the current which charges the gate capacitances to protect the GaNFETs.

The designed full-bridge rectifier circuit is implemented on a printed circuit board (PCB), see fig III, which is optimized for laboratory measurement purposes. For the final product design, the circuit can be implemented with higher power density.

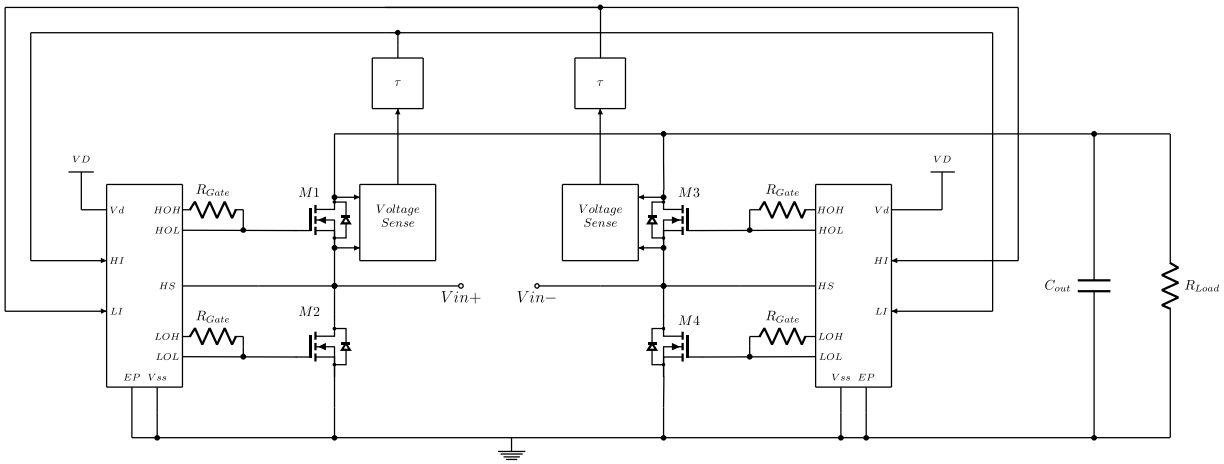


Fig. 5. Proposed Class-DE full-bridge rectifier with synchronous rectification

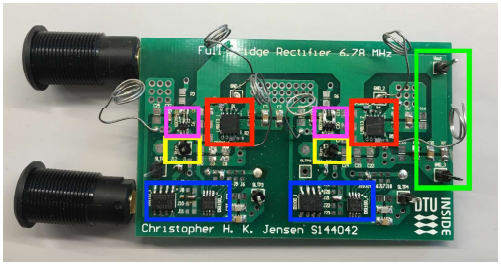


Fig. 6. Prototype PCB. Red: gate driver and GaNFETS, blue: feedback, yellow: input, pink: comparator and Green: output.

A. Impedance Matching

Impedance matching between the rectifier and the receiver coil is needed to get max power transfer at the given operating frequency.

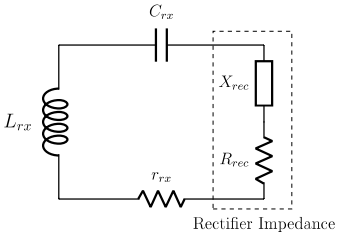


Fig. 7. Equivalent circuit for impedance matching

$$j\omega L_{rx} + \frac{1}{j\omega C_{rx}} + jX_{rec} = 0 \tag{8}$$

$$C_{rx} = \frac{1}{\omega(\omega L_{rx} + X_{rec})} \tag{9}$$

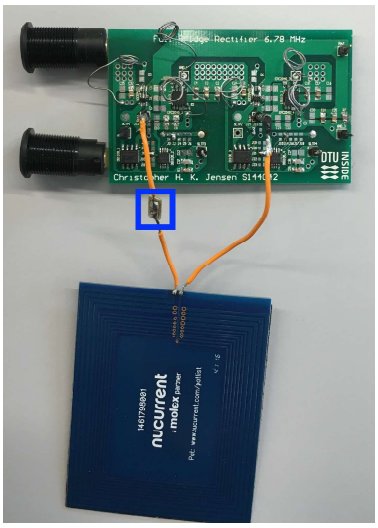


Fig. 8. Prototype with Rx. Blue: Crx

Fig. 7 shows the equivalent impedance circuit of the receiver coil and rectifier. R_{rec} and X_{rec} represents the rectifier impedance. L_{rx} and r_{rx} are the inductance and resistance of the receiver coil at the operating frequency of 6.78 MHz. At resonance the reactance should be zero and a compensation capacitor C_{rx} is added in series with the coil and rectifier to achieve resonance, see (8) and (9).

Figure III-A shows the prototype with the receiver coil, where the green PCB on top is the implemented rectifier, the blue PCB (bottom) is the Rx coil and the blue box in the middle marks C_{rx}.

The prototype full-bridge rectifier and receiving coil together with the transmitter coil and power amplifier from the EPC9112 demo kit [42] are combined to form a WPT system.

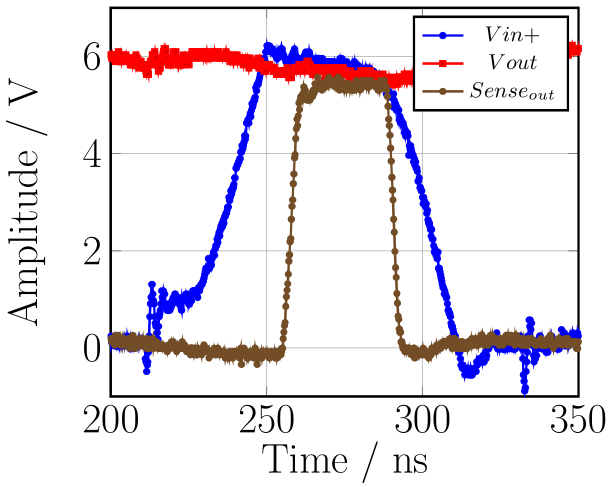


Fig. 9. Measured waveforms

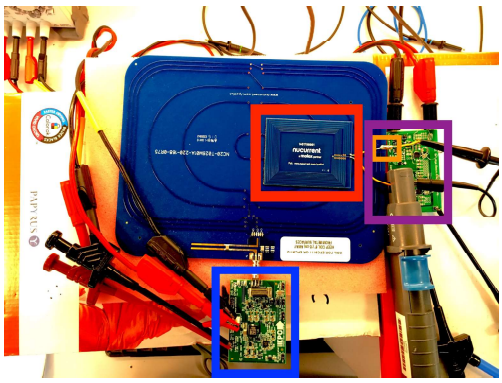


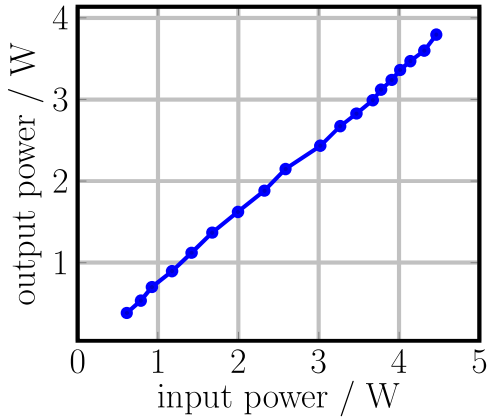
Fig. 10. Measurement setup with Tx and Rx

IV. EXPERIMENTAL RESULTS

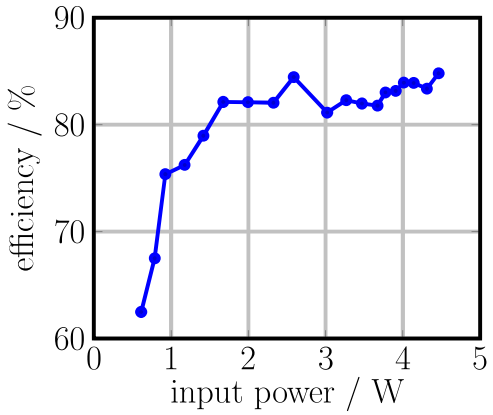
The waveforms of the prototype are verified with a LeCroy WavSurfer 104MXs-B, 1 GHx, 10 GS/s oscilloscope and for better visualization plotted in Fig. IV with the help of MATLAB. The waveform drawings in Fig. IV show the soft-switching of the power devices.

Fig. IV shows the measurement setup for the input power sweep. The red box indicates the placement of the receiving coil on top of the transmitter coil (large blue plate). The blue square in the bottom of the picture shows the power amplifier which drives the transmitter coil. On the right side the rectifier (purple box) and compensation capacitor (orange box) are shown.

The input to output power relation is linear and the efficiency of the full-bridge synchronous rectifier, which is measured with precise multimeters, is above 80 % over a wide load range. Fig. 11 shows these results. The Rx coil and circuit is arbitrarily placed on top of the Tx coil to resemble a consumer use case in the best possible way.



(a)



(b)

Fig. 11. The input output power relation and efficiency of the prototype

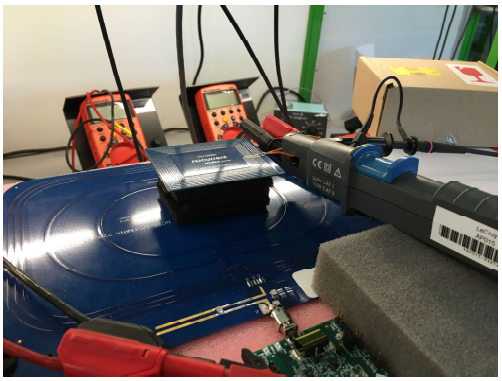
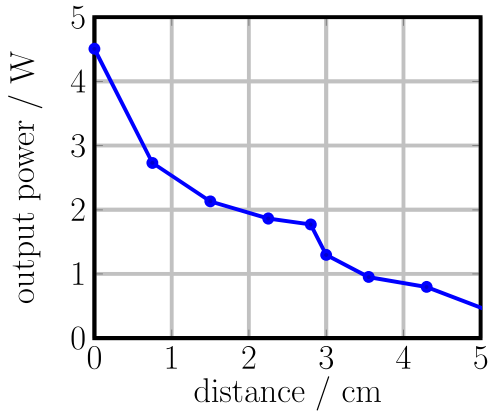
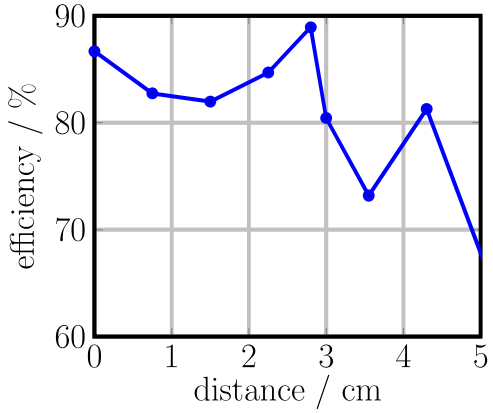


Fig. 12. Experimental setup for hight measurement

Afterwards the distance between the Tx and Rx coils is gradually increased by adding multiple 0.75 cm thick foam bricks as pictured in Fig. IV. Figure 13 is visualizing the result of this experiment. Again, the placement after each distance



(a)



(b)

Fig. 13. Output power vs receiver distance from Tx (a) and the efficiency of this (b)

change was arbitrary, which explains the roughness of the efficiency plot as a function of distance. The rectifier achieves a peak efficiency of 89 % at 3 cm distance between Tx and Rx coil.

V. Conclusion

A full-bridge Class-DE receiver circuit for wireless power transfer applications fulfilling the AirFuel standard was analyzed using component stress factors. Low voltage GaN transistors were compared using figures of merit to silicon transistors and used as synchronous rectifiers. The receiver was realized on a printed circuit board and matched to a 5 W receiver coil designed for the AirFuel operating standard. Together with a EPC transmitter base station, the receiver was implemented in a wireless power transfer system. The efficiency of the rectifier circuit is well above 80 % over a wide load range. The system was able to transmit power above 1 W over a distance of 3 cm. Future work would look into optimization of the drive circuit and a way to have the drive circuit powered from either the input or output of the rectifier.

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Appendix A-C9

Sinan Okumus, Lin Fan, Yasser Nour, and Arnold Knott, "Evaluation of custom-designed lateral power transistors in a silicon-on-insulator process in a synchronous buck converter", International Conference on Renewable Energies and Power Quality (ICREPQ'18) - Salamanca, Spain, 2018.

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Evaluation of custom-designed lateral power transistors in a silicon-on-insulator process in a synchronous buck converter

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***Abstract*—Most of todays power converters are based on power semiconductors, which are built in vertical power semiconductor processes. These devices result in limited packaging possibilities, which lead to physically long galvanic connections and therefore high external electromagnetic fields. These fields compromise power quality significantly. Therefore this paper examines the possibility to use lateral silicon-on-insulator power MOSFETs and uses the custom-made devices in a $48\ \mathrm{V}$ to $12\ \mathrm{V}$ synchronous buck converter in continuous conduction mode. The converter is designed based on custom made power transistors, implemented and verified by experimental results. The resulting efficiency of the $1\ \mathrm{W}$ converter is around $93\ \%$ across a wide load range and its temperature rise is less the $10\ ^{\circ}\mathrm{C}$. This leads to the conclusion, that modern lateral silicon-on-insulator power processes allow high integration of power stages and therefore promise lower emissions, leading to higher power quality.**

***Index Terms*—power semiconductors, vertical semiconductor process, lateral semiconductor process, silicon-on-insulator process, buck converter**

I. Introduction

Modern power semiconductor transistors are often constructed as vertical devices. [1]–[3] The advantage of vertical devices are very low on-resistances $R_{DS_{on}}$ in combination with low gate charges Q_g, therefore resulting in a low figure of merit FOM, where $FOM = R_{DS_{on}} \cdot Q_g$. The FOMs of several processes can be compared to each other for a given maximum device voltage, as a bigger gate area increases the width of the channel, therefore effectively reducing its $R_{DS_{on}}$, but negatively affecting the gate charge Q_g due to the increased plate areas of the gate facing the channel. These plates effectively create the input capacitance C_{iss} and represent the gate charge Q_g.

Within all other integrated circuit design areas, such as Complementary Metal Oxid Semiconductors (CMOS), such as [4]–[7], lateral devices are state-of-the-art. Figure 1 shows a simplified representation of a vertical and a lateral Metal Oxid Semiconductor Field Effect Transistor (MOSFET).

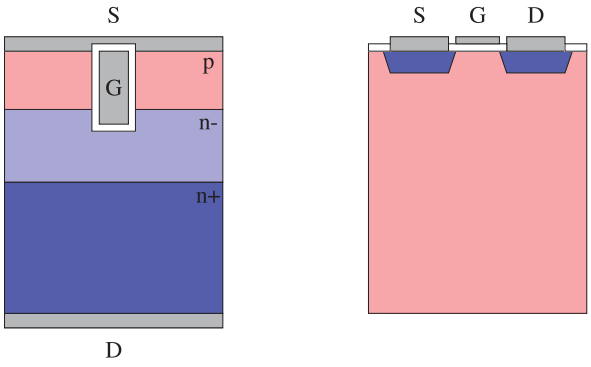

Fig. 1. Simplified example of crosssection of the die of a vertical (left side) and a lateral (right side) power n-channel MOSFET, where D is drain, G is gate and S is source. The coloring and n+, n- and p are indicating the doping of the semiconductor. The bulk connection in the lateral device is neglected.

The vertical n-channel device on the left side of Fig. 1 is using the whole die thickness and the n-doped wafer provides plenty of electrons to be flushed into the channel, when attracted by a positive potential applied between gate (G) and (S) source, hence a low resistance between drain (D) and source (S), i.e. low $R_{DS_{on}}$.

The lateral device on the right side of Fig. 1 is built on a p-doped wafer, where the number of free electrons to be attracted to the channel between drain (D) and and source (S) are rather low. However in this case, the backside of the die - called bulk (B) - has no electrical function and is typically tied to the lowest potential of the implemented circuit, which is the

source of the power MOSFET in this case.
For building a power stage, many power converter topologies, such as synchronous buck, synchronous boost, half-bridge and full-bridge, require two stacked power transistors. These stacked power transistors are the power stage inside those topologies and are called half-bridge or switching pole. Figure 2 shows such a half-bridge configuration.

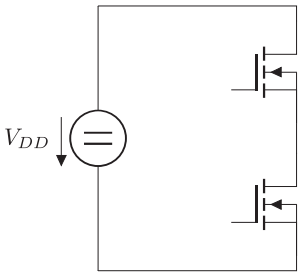

Fig. 2. Half bridge switch-mode power stage realized with two n-channel MOSFETs.

When connecting two vertical MOSFETS in such a half-bridge configuration, the top-metallization of the low-side device is connected to ground and the backside metallization of the other die is connected to the supply voltage V_{DD}. Furthermore, the backside of the die of the low-side MOSFET needs to be shorted to the topside of the high-side MOSFETs die. This node is the switch node, which is carrying a high $\frac{dI}{dt}$ and $\frac{dV}{dt}$. Figure 3 is visualizing these connections.

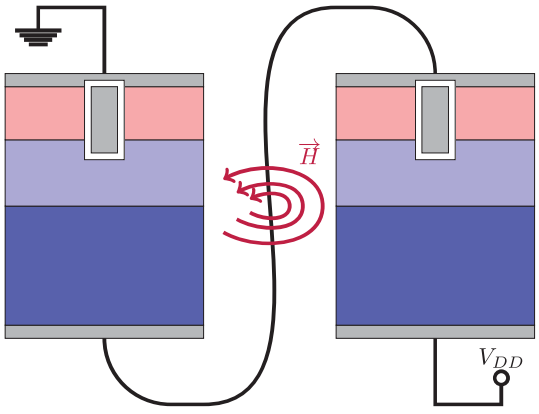

Fig. 3. Parasitics inductance and resulting magnetic field through connection of two vertical MOSFETs in a half bridge configuration

Especially the $\frac{dI}{dt}$ running in this connection generates a magnetic field $\vec{H}$, which is defined by equation 1:

$$\vec{H} = \oint \frac{dI}{dt} dl. \tag{1}$$

If the path l, which the alternating current (AC) is flowing along, is long, the area between the forward and the return path of the loop is big and therefor the integral on the right side of the equation is big.
In the case of vertically implemented MOSFETs, the physical path, where this current flows is rather large, as it consists of a number of mechanical connections:

- drain connection of die of low-side device
- package
- printed circuit board
- source pin of high-side device
- lead frame of high side device
- source bonding wire of high-side device
- routing in metal of high-side source

Therefore the resulting $\vec{H}$-field is rather big, which results in a significant contribution to radiated electromagnetic emissions, which can potentially couple into other circuits in the same system [8] or even worse getting emitted outside the mechanical enclosure of the system. This compromises the radiated electromagnetic compatibility (EMC) significantly and therefore compromises the power quality of the system.
When connecting lateral power devices in a half-bridge configuration as provided in Fig. 2, the high-side device needs to be isolated from the die-substrate, the bulk, which is accomplished by modern silicon-on-insulator processes (SOI). Such an arrangement is visualized in figure 4.

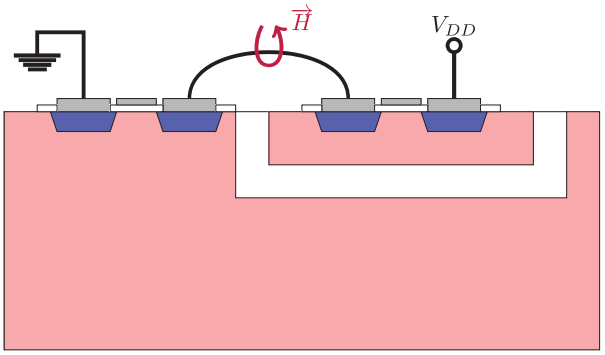

Fig. 4. Parasitics inductance and resulting magnetic field through connection of two lateral MOSFETs in a half bridge configuration

Compared to the routing of the switch-node in vertical devices, the alternating current in the lateral configuration only needs to be routed inside the metallization layers on top of the active silicon and does neither leave the package nor the die. Therefore the forward and the return path of the loop, penetrated by the alternating current is rather short, resulting in a significantly reduced $\vec{H}$-field.
As initially mentioned, the increased on-resistance of the vertical devices compared to the vertical counterparts, is their largest drawback. Therefore this paper focuses on the usability of lateral devices in power converters with respect to achievable efficiency. Section II introduces the custom made lateral SOI devices used in section III in a synchronous buck

converter design. Section IV shows the achieved experimental results and section V concludes the paper.

II. Custom made lateral power devices in silicon-on-insulator process

The design procedure and layout extracted results for the four designed lateral power MOPSFETs in a 180 nm SOI high voltage process is given in [9] and [10]. The resulting on-resistances of the two bigger devices are in the 2.5 Ω-range and the two smaller devices achieve around 3 Ω. Figure 5 provides the top-view of the designed devices, revealing their aspect ratio and their relative sizes. Furthermore, the bonding diagram is included in Fig. 5.

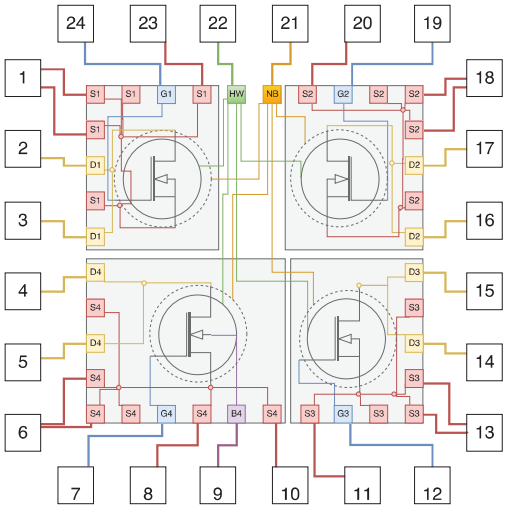

Fig. 5. Bonding diagram and top-view of the layout of the test MOSFETs

Figure 6 shows the packaged devices with open lid after soldering on a test printed circuit board (PCB). Here the aspect and size ratio of the two uper MOSFETs compared to both lower MOSFETs is even more visual, corresponding to the approximately 0.5 Ω difference in on-resistance between the respective drain and source connections, when the gate-source voltage is above the devices threshold voltage.

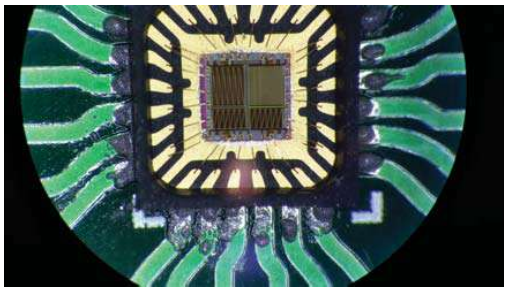

Fig. 6. Die photograph, when mounted on a printed circuit board (PCB).

III. Design of synchronous buck converter

The synchronous buck converter is designed to fullfil the specifications given in table I.

TABLE I
Specifications for synchronous buck-converter based on the SOI MOSFETs

Parameters	Value
Input Voltage V_{in}	48 V
Output Voltage V_{out}	12 V
Maximum output power $P_{out_{max}}$	$\geq$ 1 W
Switching frequency f_{sw}	100 kHz
Output voltage ripple ΔV_{out}	$\leq$ 500 mV
Operation mode	continuous at $P_{out_{max}}$

These specifications result in an output current I_{out} of

$$I_{out_{max}} = \frac{P_{out_{max}}}{V_{out}} = 83 \text{ mA}, \tag{2}$$

which results in an equivalent load resistance R_{load} of

$$R_{load_{min}} = \frac{V_{out}}{I_{out_{max}}} = 144 \ \Omega. \tag{3}$$

To keep the converter in continuous conduction mode [11] at the maximum power level $P_{out_{max}}$, the output inductor L_{out} must fullfil

$$L_{out} \geq \frac{(1-d)R_{load_{min}}}{2 \cdot f_{sw}} = 540 \ \mu\text{H}, \tag{4}$$

where d is the duty cycle of the buck converter in continuous conduction mode, derived as $d = \frac{V_{out}}{V_{in}} = 0.25$. The 820 µH inductor MSS1278-824KL with ± 10 % tolerance and a maximum series resistance of 1.296 Ω from Coilcraft satisfies the design criteria. The contribution of the inductors DC resistance to the losses in the converter is therefore limited to 9 mW and an inductor ripple current $\Delta I_{L_{out}}$ of

$$\Delta I_{L_{out}} = \frac{(1-d)V_{out}}{f_{sw} \cdot L_{out}} = 110 \text{ mA}. \tag{5}$$

The contribution of the switching losses of the inductor are estimated in the approximate same range to 10 mW.
To keep the output ripple within the requirement an output capacitor C_{out} of

$$C_{out} \geq \frac{\Delta I_{L_{out}}}{4 \cdot f_{sw} \cdot \Delta V_{out}} = 550 \text{ nF} \tag{6}$$

is needed, where the design choice for C_{out} is a 590 nF ceramic X7R capacitor with 50 V rating. The losses in the equivalent series resistance of the output capacitor are negligible.
The half-bridge needs a gate driver. Here the design choice is an L5113 with a maximum power dissipation of 15 mW.
The completed design results in full schematic in Fig. 7 including all decoupling capacitors and the inputs to the gate driver.

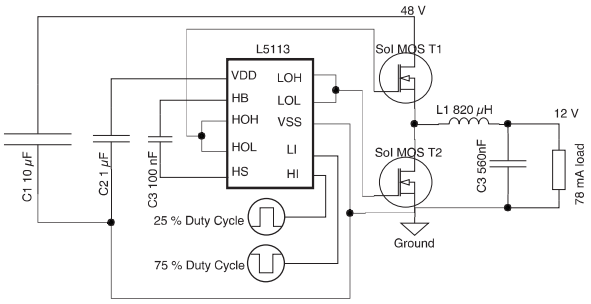

Fig. 7. Total schematic of the implemented synchronous buck converter.

Figure 8 shows a picture of the implemented prototype.

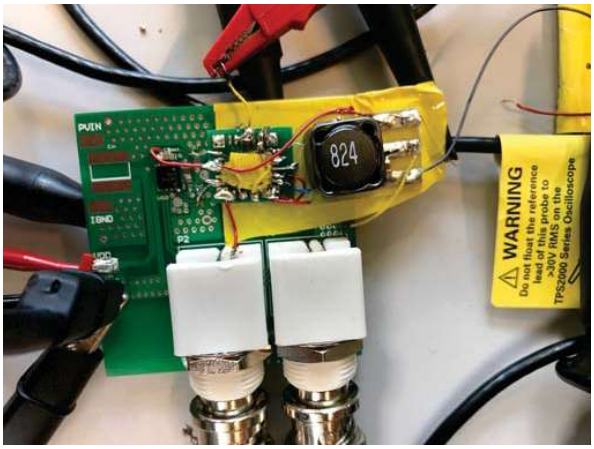

Fig. 8. Photograph of the implemented synchronous buck prototype with the test chip under yellow isolation take, the gate drive signals fed through the white BNC connectors at the bottom and the output inductor on the right side.

IV. Experimental Results

The block diagram of the experimental verification setup is provided in Fig. 9.

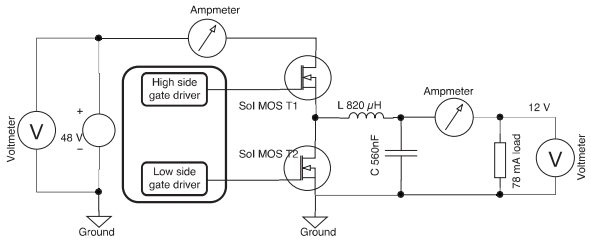

Fig. 9. Block diagram of setup to verify the usability of lateral SOI-based MOSFETs in the designed synchronous buck converter.

Figure 10 shows the laboratory setup, where the function generator Rigol DG4062 provides the gate signals and the active load ELA250 from Zentro Elektrik functions as the load resistor.

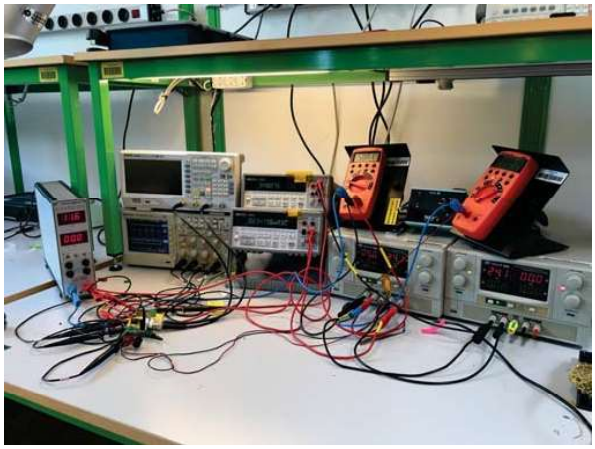

Fig. 10. Photograph of laboratory setup including - from left to right - the active load, the prototype, the function generator, the multimeters and the supplies for the input voltage as well as the auxiliary supply for the gate driver.

The correct operation of the buck converter is confirmed by measuring the switch node, e.g. the connection of the low-side MOSFETs drain to the high-side MOSFETs source, while monitoring the output voltage. Fig. 11 shows a screenshot of the oscilloscope measurement. The output voltage V_{out} is 12.0 V, the average voltage of the switching node is 12.5 V, while the converter is operating at 100.0 kHz. The overswing on the switch-node are an artifact of the applied measurement technique, resulting from the coupling of magnetic fields into the loop of the ground clip of the oscilloscopes probe.

Fig. 11. Verification of the operation of the synchronous buck converter based on custom made lateral SOI power MOSFETs. From top to bottom: output voltage (green, 2 V/div), switch node (purple, 20 V/div), low-side input to the gate driver (cyan, 5 V/div) and its high-side input (yellow, 5 V/div) with a time base of 5 $\mu\mathrm{s}/div$

The most important parameter to verify the usability of lateral power MOSFETs in switch-mode power stages to reduce the

external fields and therefore improve the overall power quality of the converter is its achievable efficiency. The losses in the passive components, i.e. the output inductor and the output capacitor, as well as the losses in the gate drive are minimized by design. This leaves the switching and conduction losses in the power devices as the determining factor of efficiency, as the parasitic capacitances of the power devices are responsible for the switching losses and the on-resistance dominates the conduction losses. Hence the definition of the FOM. Figure 12 represents the final quantitive representation of the losses in the converter.

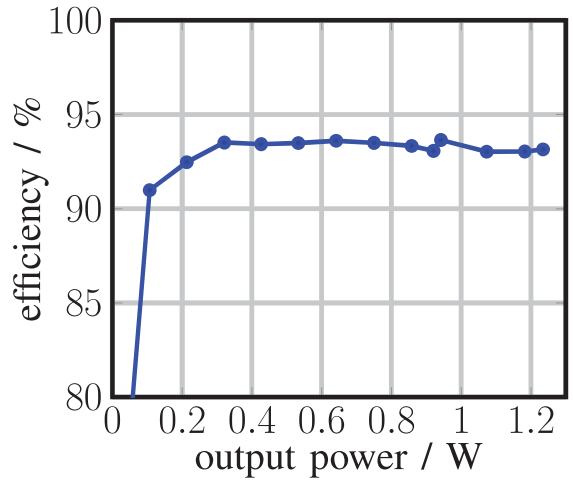

Fig. 12. Measured efficency of the implemented buck converter

Over a wide power range (from 10 % of $P_{out_{max}}$ to $P_{out_{max}}$), the converter operates above 90 % and at more than 300 mW the efficiency is around 93 %. This leaves about 70 mW to losses, of which 34 mW have been accounted for in the gate driver (15 mW) and the output inductor (19 mW) by design above. The remaining 36 mW of losses are expected in the power semiconductors.

The thermal image of the converter confirms the power semiconductors as the highest components with the highest temperature. Given their physical volume and the fact that they dissipate about half of the total losses, this is expectable. As the highest temperature of the converter in thermal equilibrium is 34.6 °C, only 8.9 °C above the ambient temperature of 25.7 °C, the overall performance of the converter is acceptable for many applications. Given a maximum operating temperature of silicon devices at 150 °C and adding a small safety margin, this design can be qualified up to an ambient temperature of 140 °C, which is enough for most consumer, industrial, automotive and space applications.

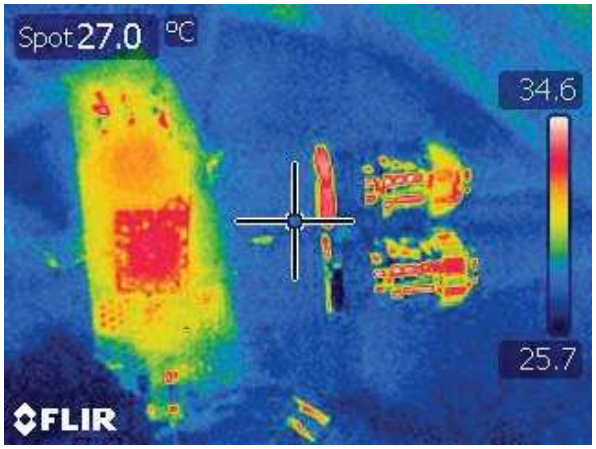

Fig. 13. Thermal image of the synchronous buck converter under operation: the highest temperature rectangle to the left of the cursor represents the tested custom made lateral SOI power MOSFETs, whereas the hot spots to the right of the cursor are the BNC connectors - which might represent a wrong temperature due to the reflective nature of their surface with respect to the infrared cameras measurement technique.

V. Conclusion

Lateral power semiconductors are proposed as a method to reduce emitted magnetic fields compared to the widely used vertical power devices. To check the feasibility of the lateral devices, their useability in power converters needs to be examined. This paper used custom made silicon-on-insulator lateral power MOSFETs to determine the applicability of the selected process in power electronics. A 48 V to 12 V, 1 W synchronous buck converter was designed and experimentally verified. The experimental results show a high efficiency (around 93 %) over a wide load range and a temperature rise of less than 10 °C, proofing that lateral silicon-on-insulator power MOSFETs are a serious alternative to vertical devices.

Acknowledgements

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